

Compal confidential

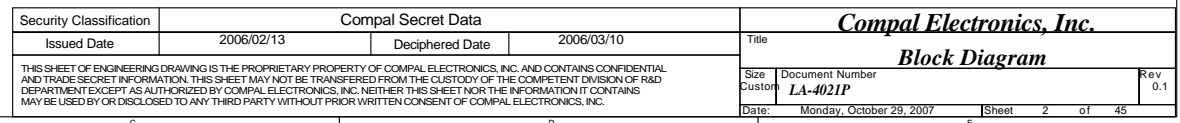
Schematics Document

Mobile Penryn uFCPGA with Intel
Cantiga_GM+ICH9-M SFF core logic

SKYY
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2007-10-26


Security Classification		Compal Secret Data		Title	
Issued Date	2006/02/13	Deciphered Date	2006/03/10	Cover Sheet	
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Voltage Rails (O MEANS ON X MEANS OFF)

power plane State	+B	+5VALW +3VALW +3VM +1.05VM	+1.8V	+5VS +3VS +1.5VS +0.9V +VCCP +CPU_CORE +0.9V
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Symbol Note :

 : means Digital Ground

 : means Analog Ground

@ : means just reserve , no build
CONN@ : means ME part.
45@ : means install after SMT.

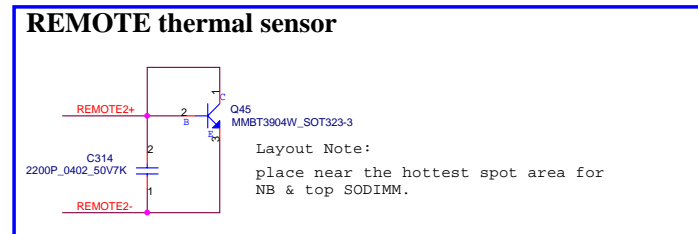
SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU)	SODIMM	CLK CHIP	MINI CARD	LCD
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X
SMB_CK_CLK1 SMB_CK_DAT1	ICH9	X	X	X	X	V	V	V	X
LCD_CLK LCD_DAT	Cantiga	X	X	X	X	X	X	X	V

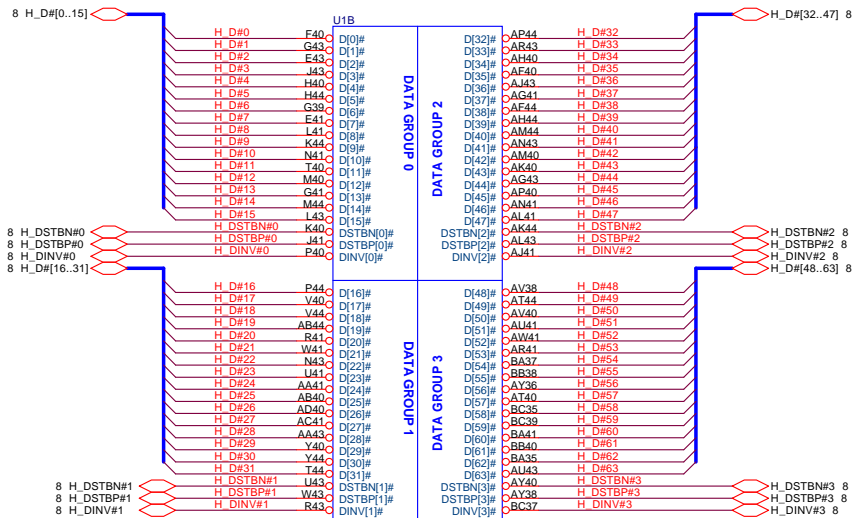
I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

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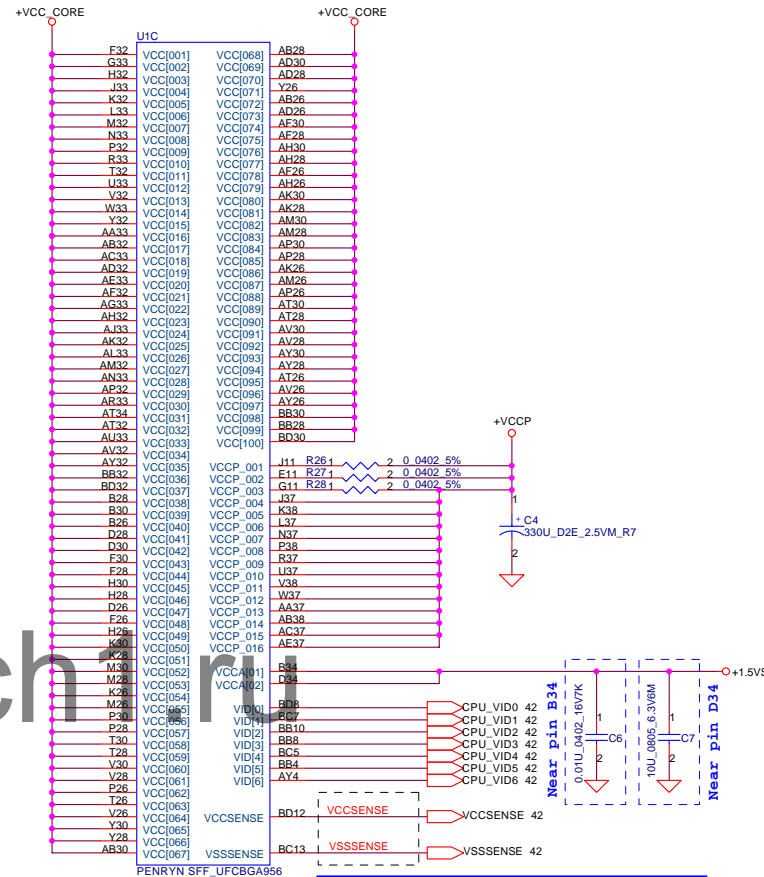
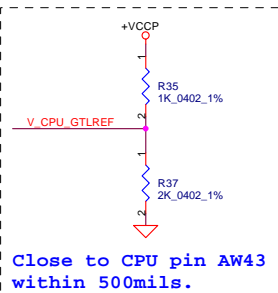
Security Classification		Compal Secret Data		Compal Electronics, Inc. Penryn(1/3)-AGTL+/ITP-XDP		
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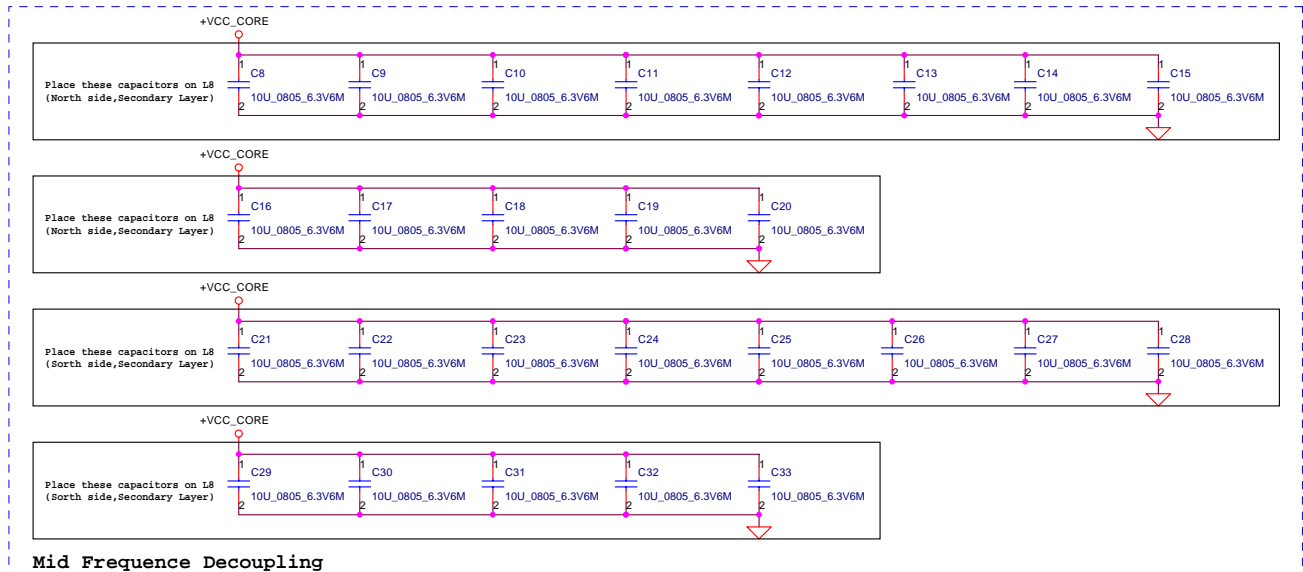
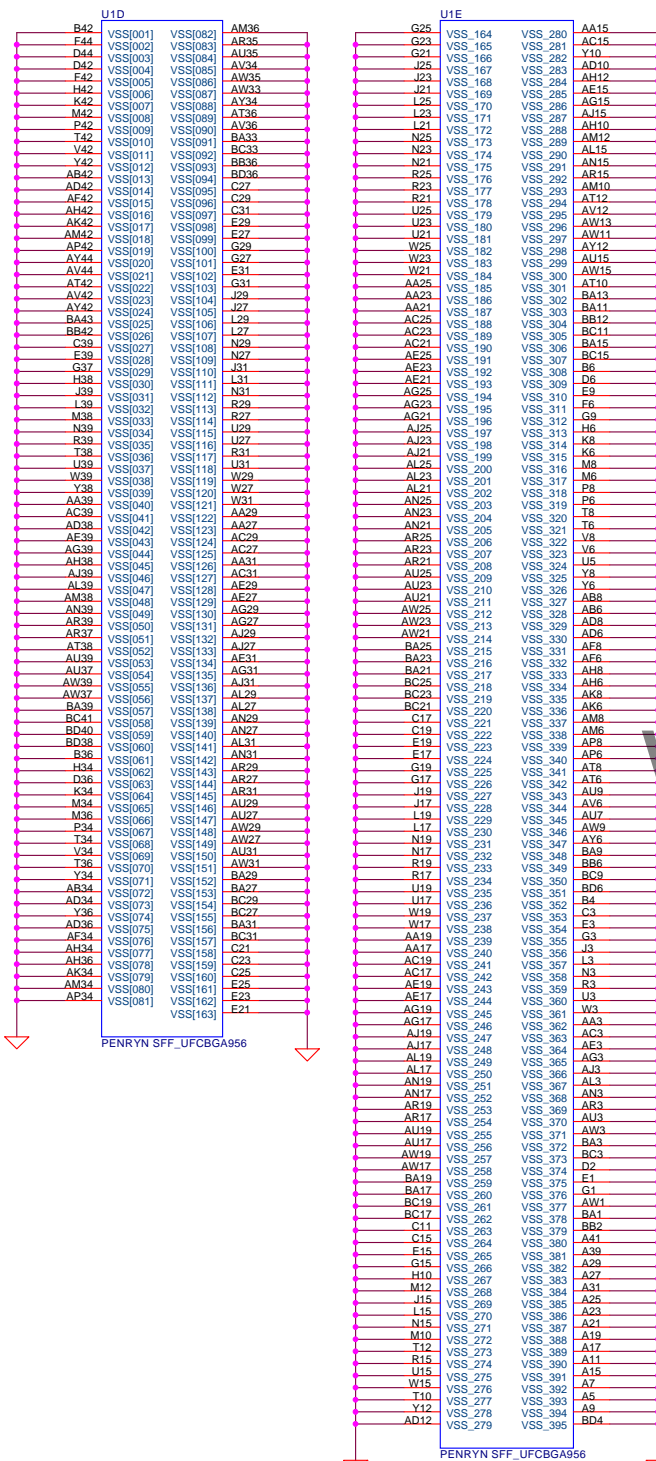
layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0

Resistor placed within 0.5" of CPU pin.Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.

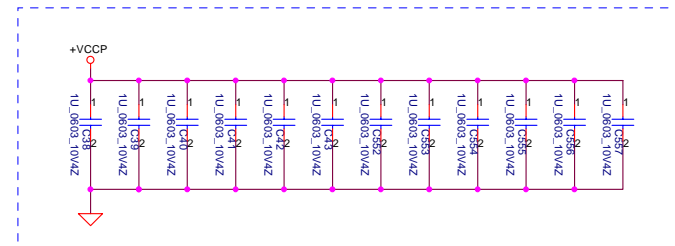
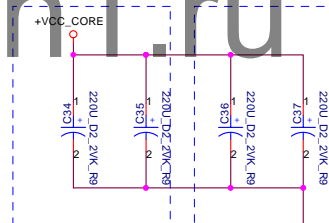


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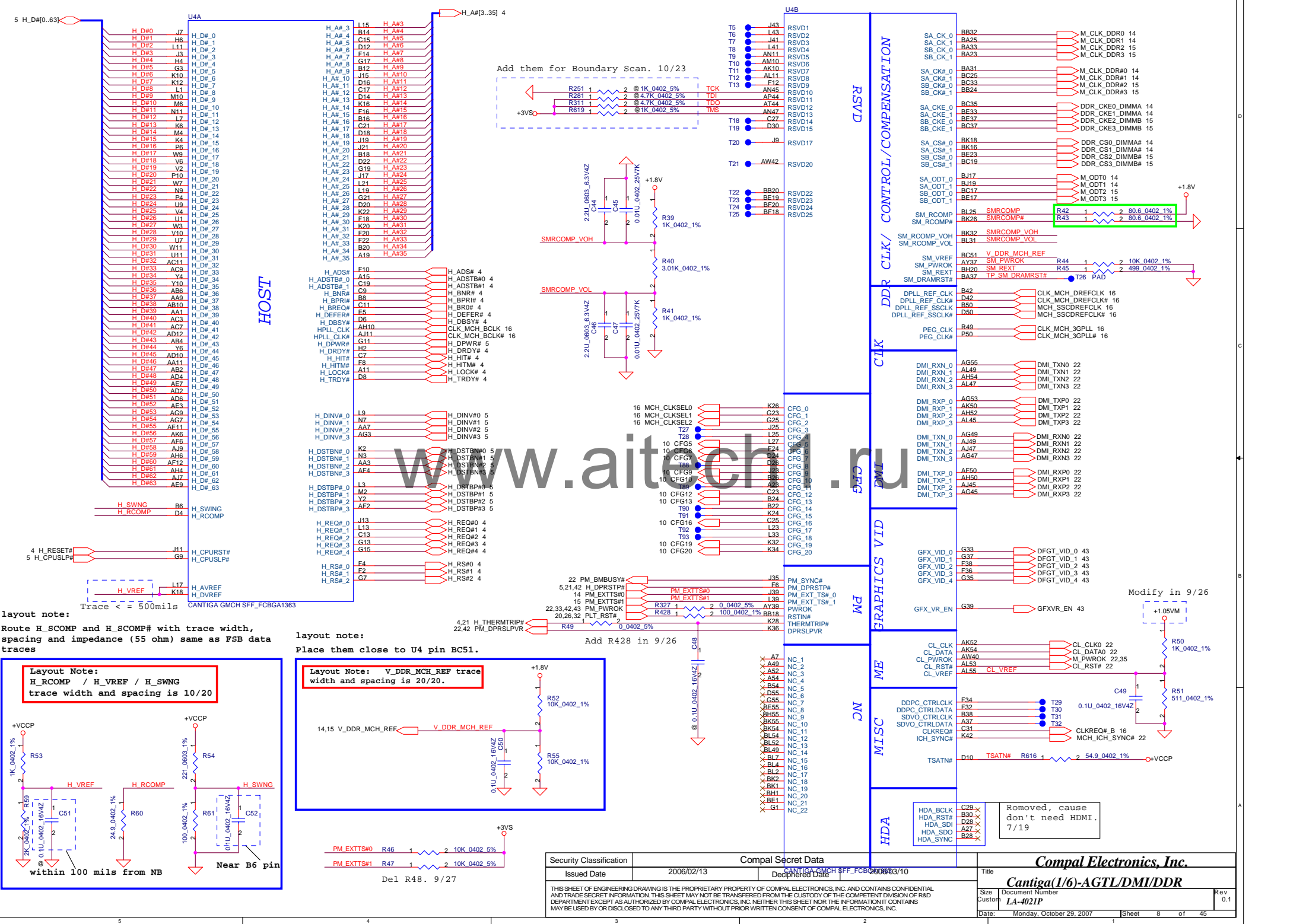


Near CPU CORE regulator

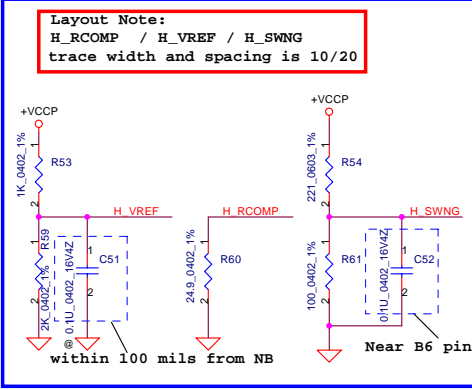
ESR <= 1.5m ohm



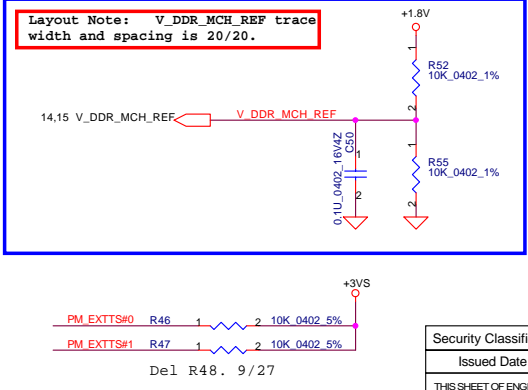
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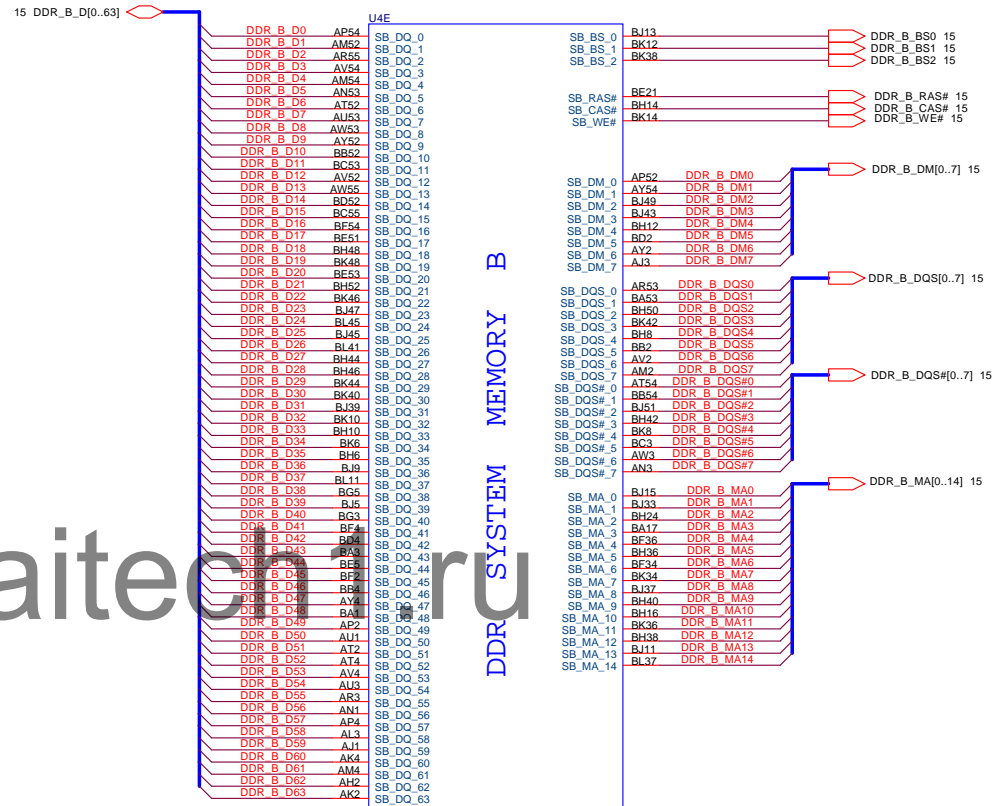
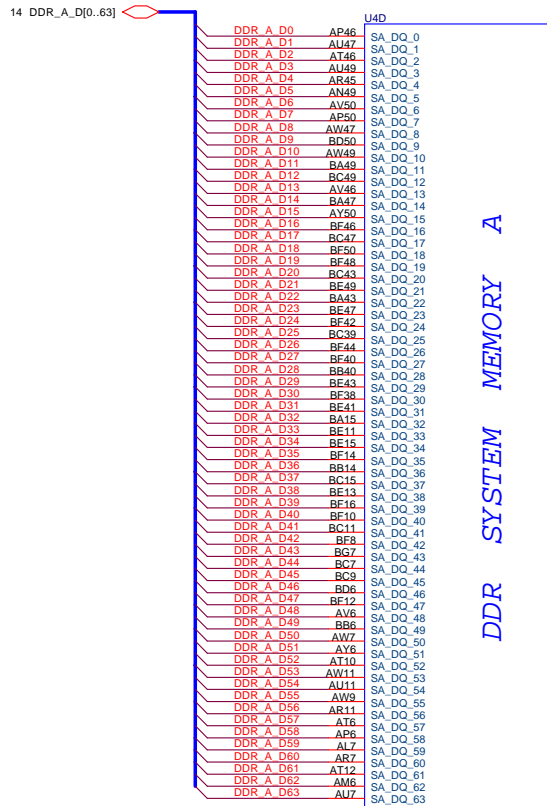
layout note:
Route H_SCOMP and H_SCOMP# with trace width, spacing and impedance (55 ohm) same as FSB data traces



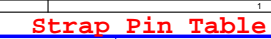
layout note:
Place them close to U4 pin BC51.

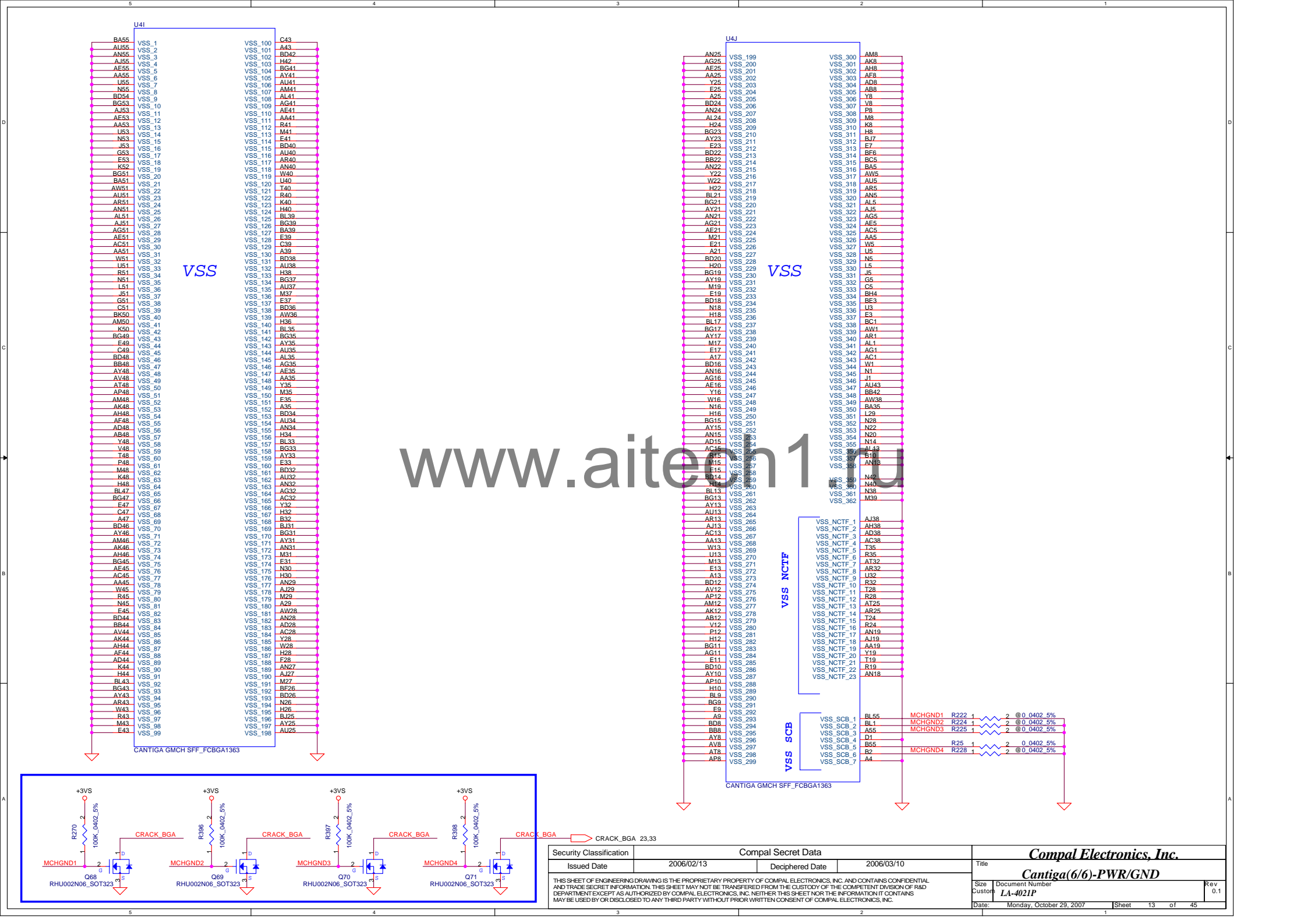


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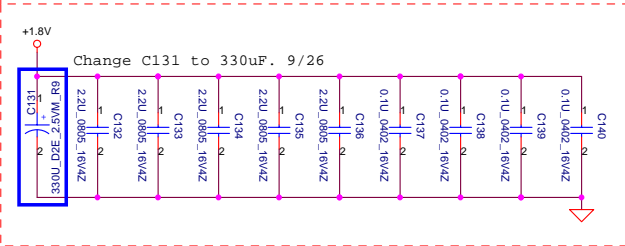
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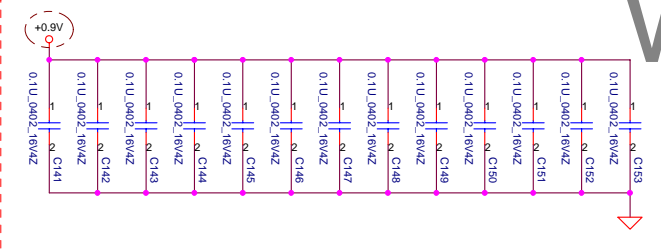


9 DDR_A_DQS#[0..7]
9 DDR_A_D[0..63]
9 DDR_A_DM[0..7]
9 DDR_A_DQS[0..7]
9 DDR_A_MA[0..14]

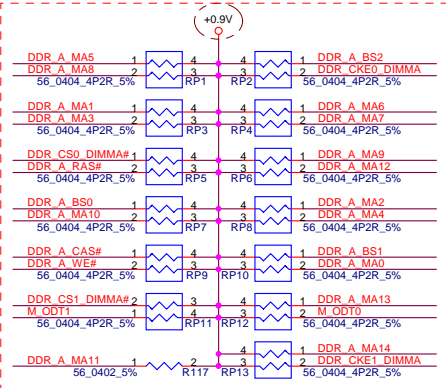
Layout Note:
Place near JP36



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V



Layout Note:
Place these resistor closely JP9, all trace length Max=1.5"



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9 DDR_B_DQS#[0..7]

9 DDR_B_D[0..63]

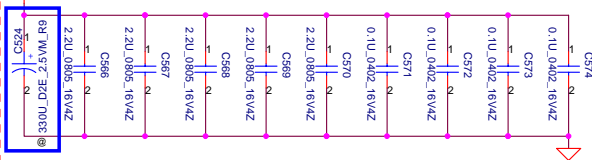
9 DDR_B_DM[0..7]

9 DDR_B_DQS[0..7]

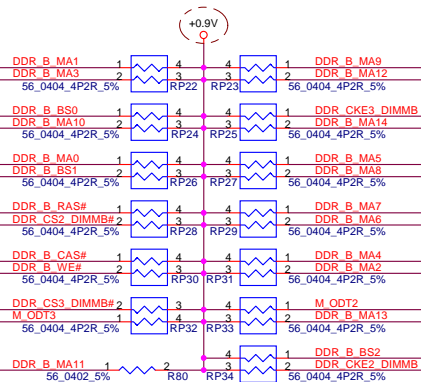
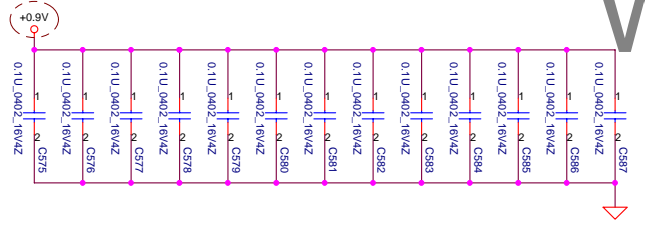
9 DDR_B_MA[0..14]

Layout Note:
Place near JP34

+1.8V Reserve C524. 9/26

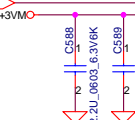


Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V



Layout Note:
Place this resistor closely JP10,all trace length Max=1.5"

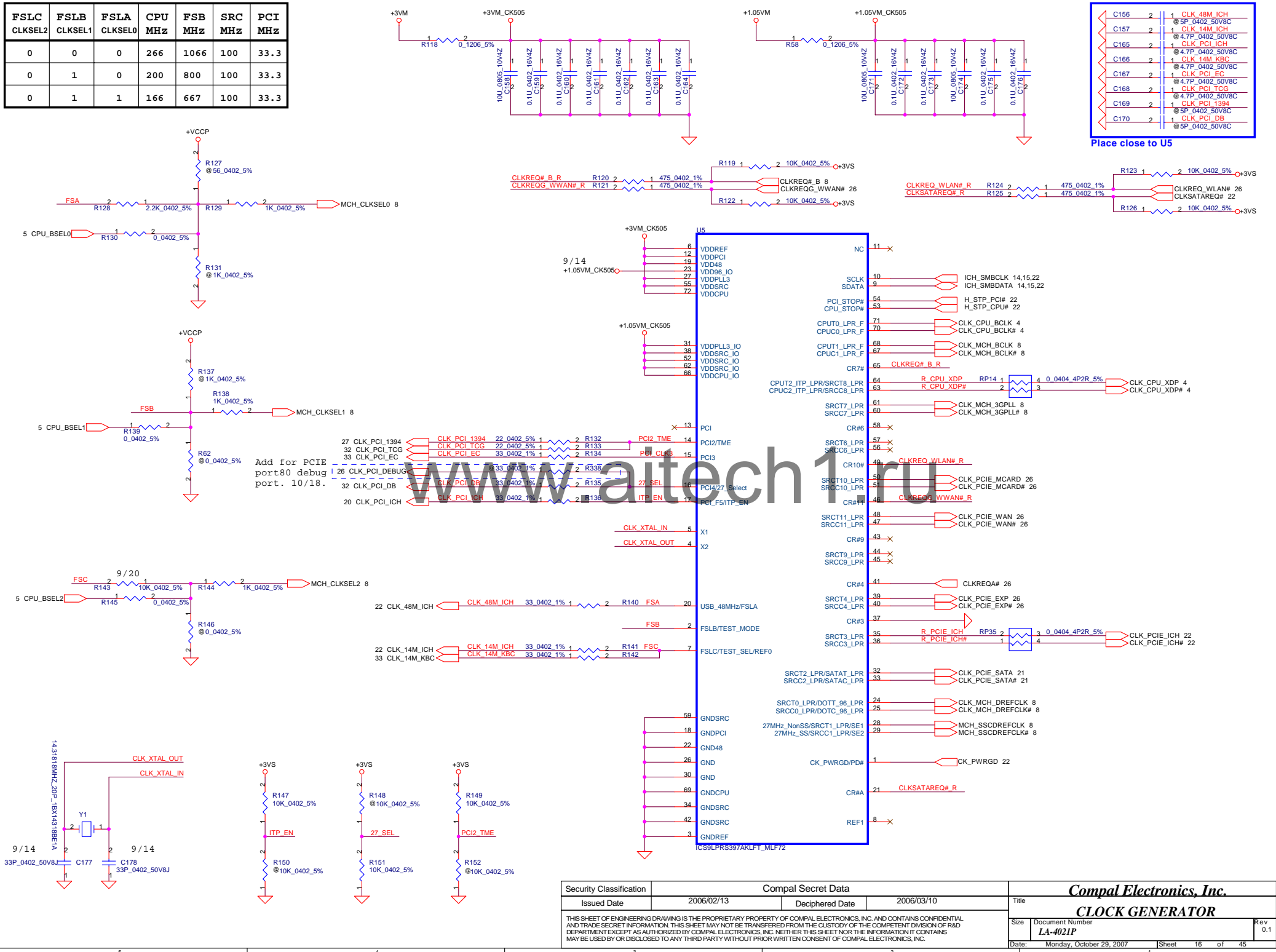
14,16,22 ICH_SMBDATA
14,16,22 ICH_SMBCLK



SO-DIMM B
REVERSE
Bottom side

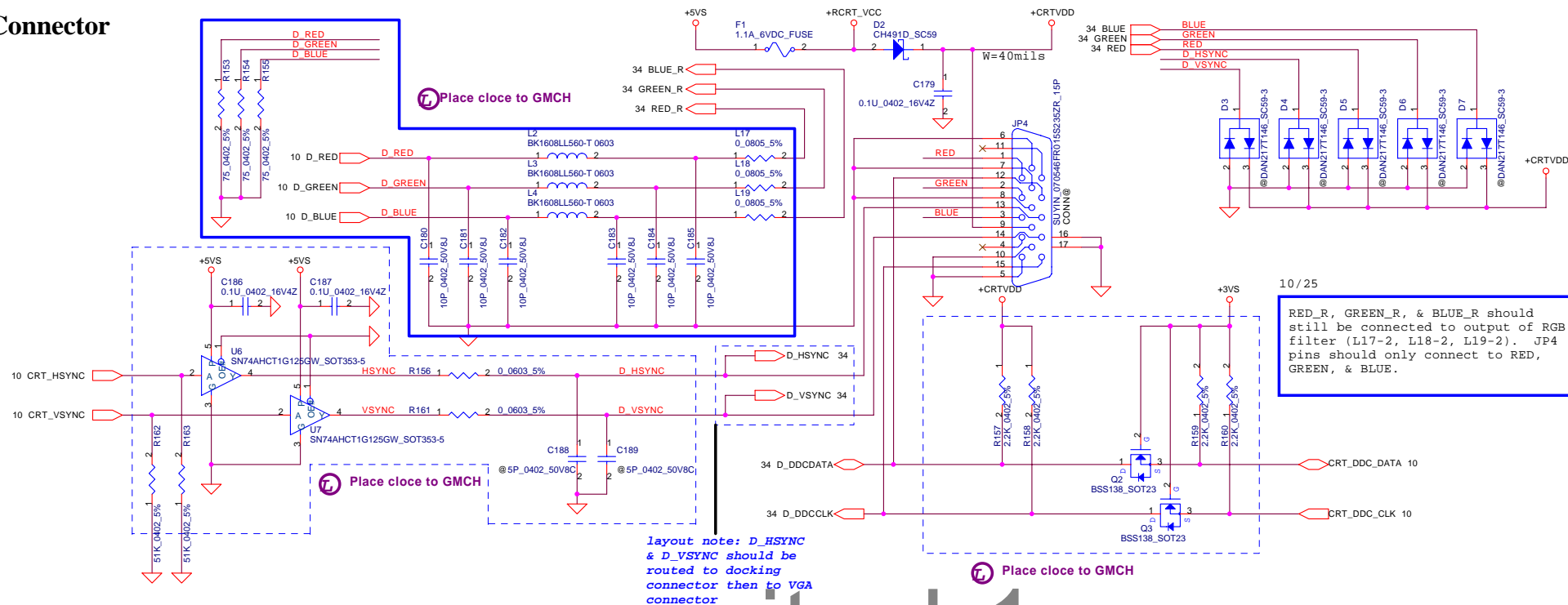
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FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	FSB MHz	SRC MHz	PCI MHz
0	0	0	266	1066	100	33.3
0	1	0	200	800	100	33.3
0	1	1	166	667	100	33.3



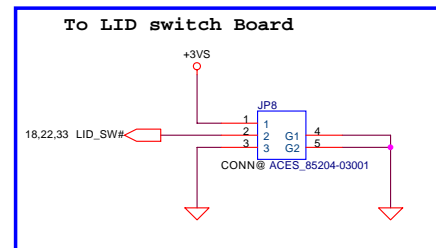
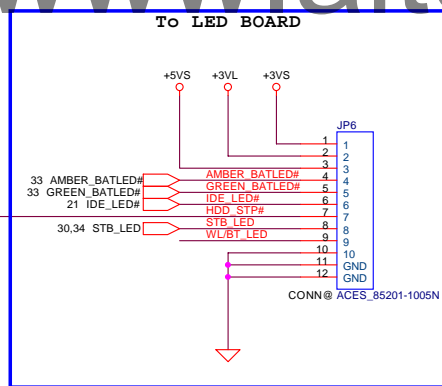
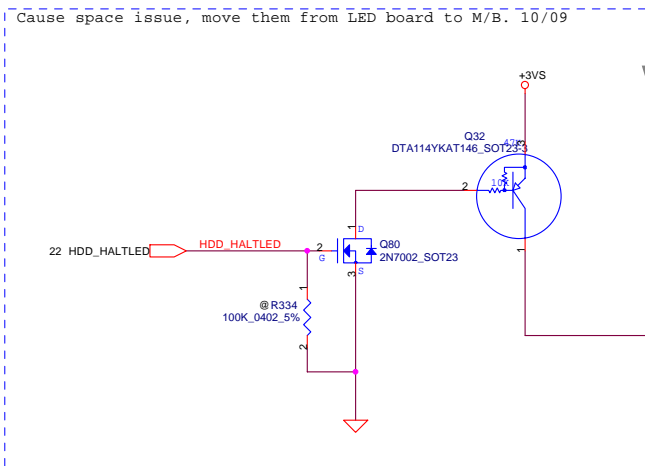
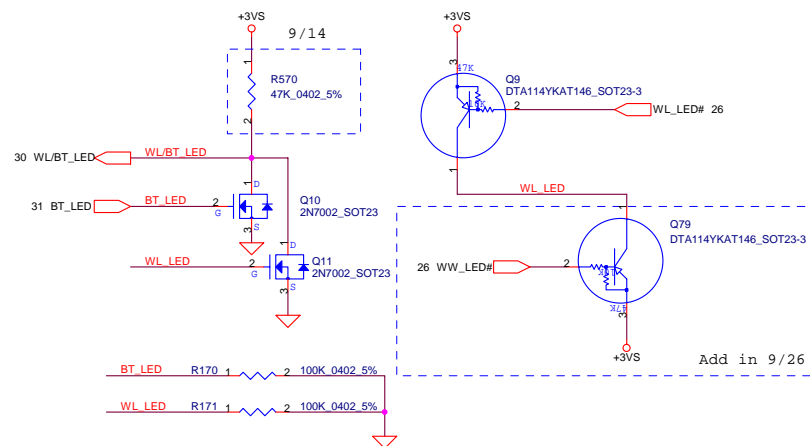
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CRT Connector

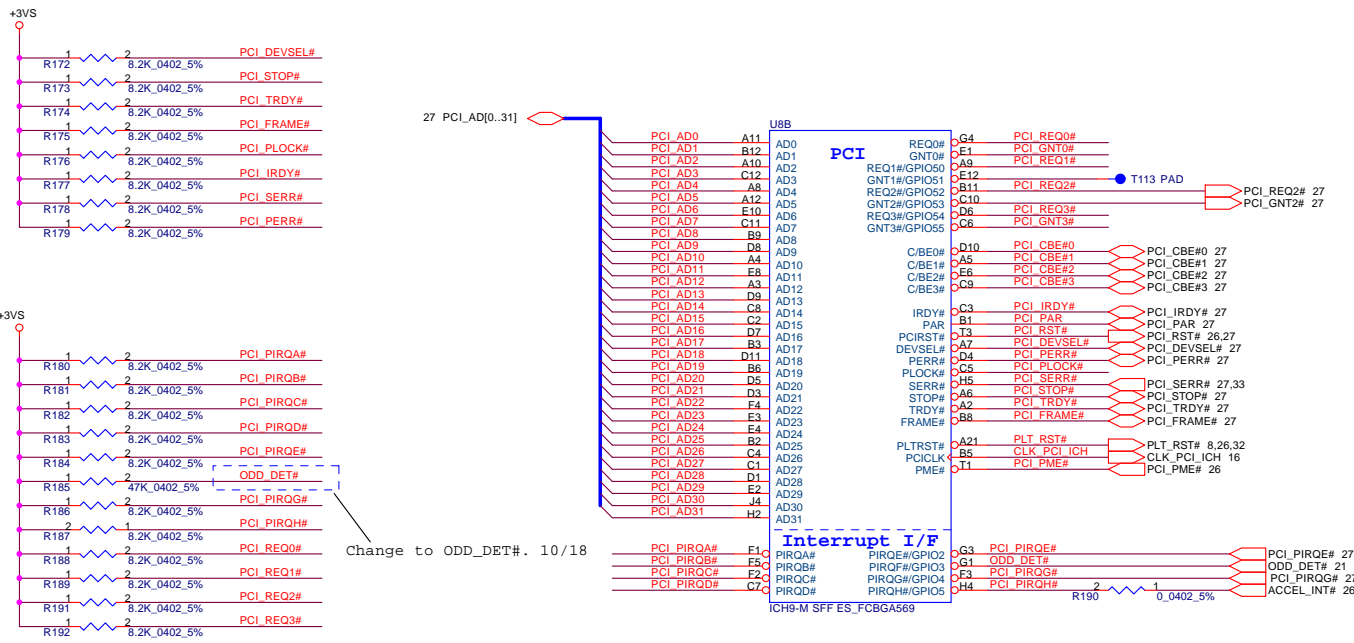


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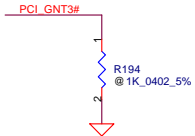


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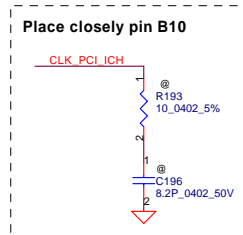
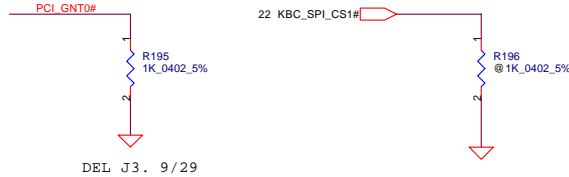


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A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enble High= Default *

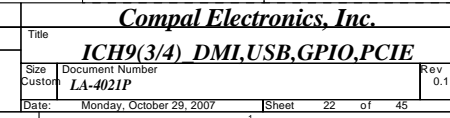


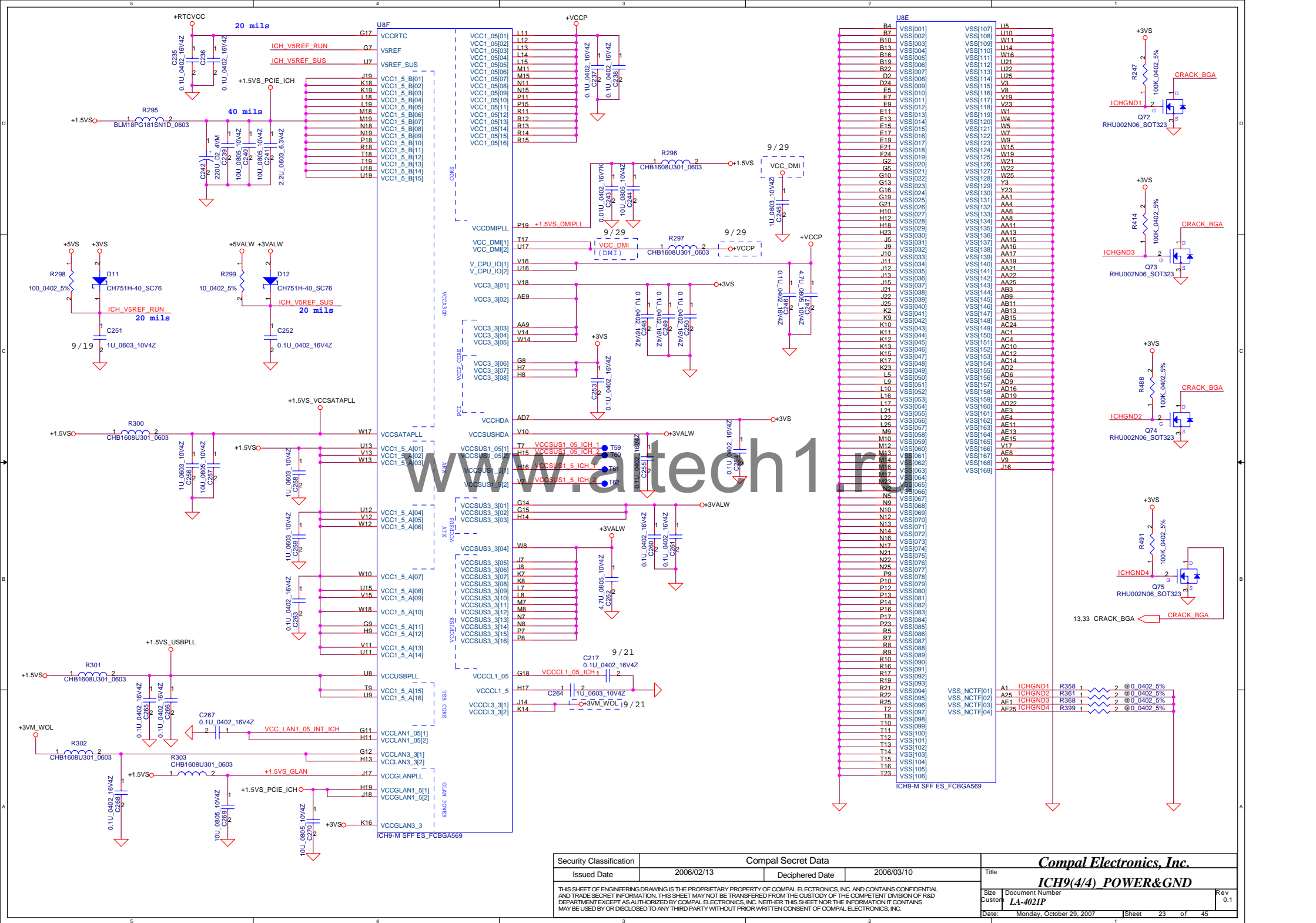
Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI *
1	0	PCI
1	1	LPC



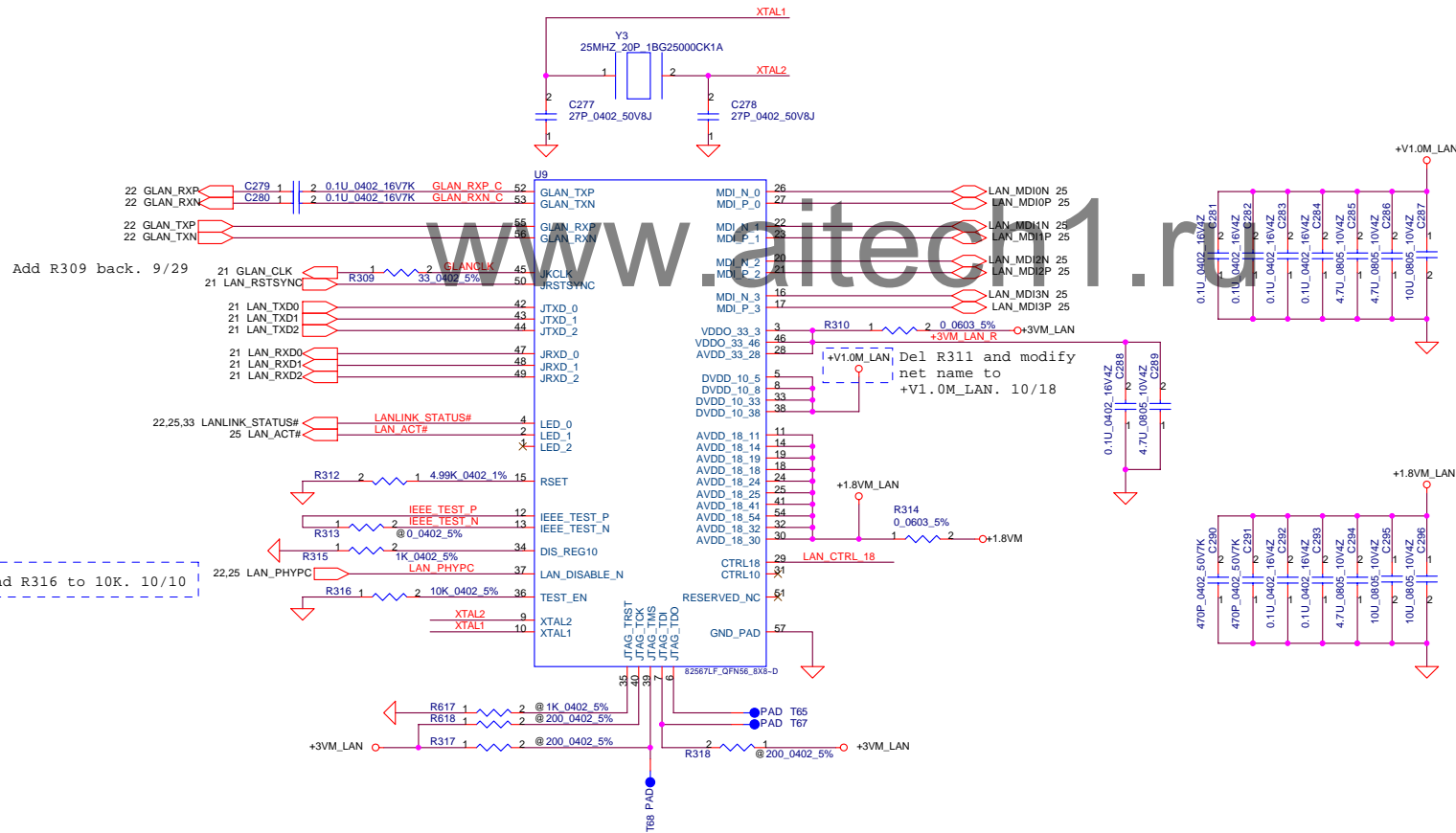
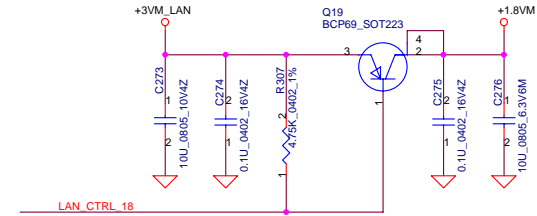
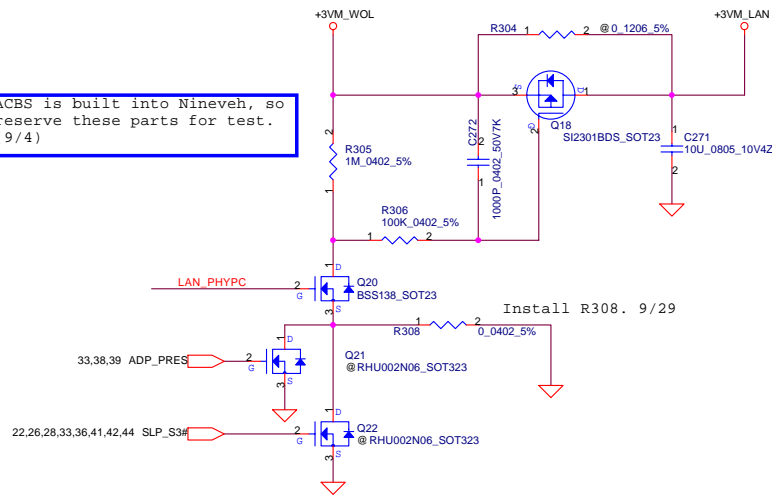
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Security Classification	Compal Secret Data			<i>Compal Electronics, Inc.</i>		
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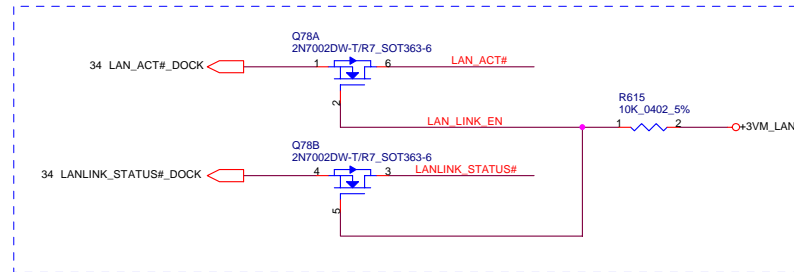
ACBS is built into Nineveh, so reserve these parts for test.
(9/4)



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Del LAN ENERGY DET cause already inside the BOAZ. 9/27

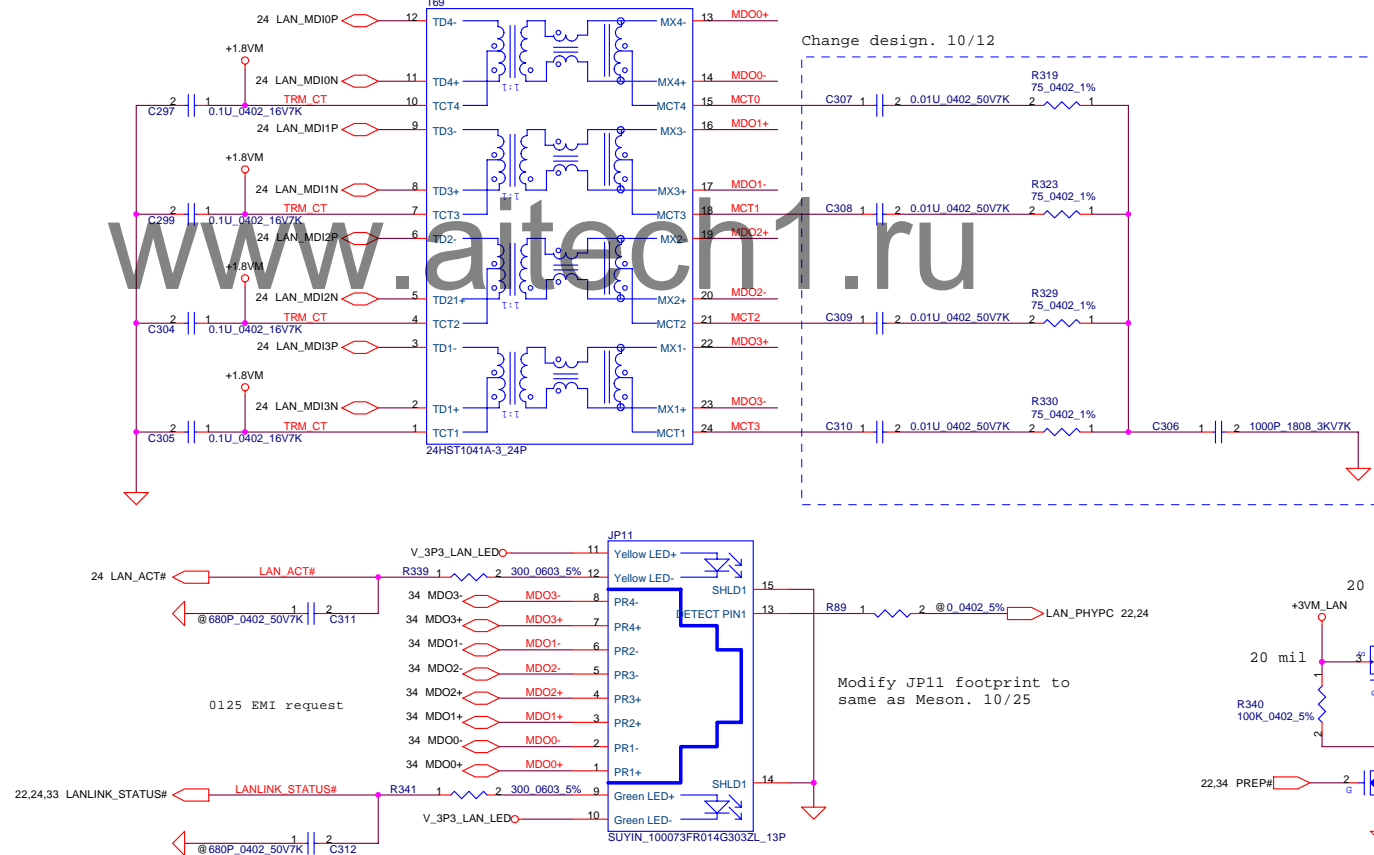
LAN status/link level shift. 9/21



Delete all termination cause they are already inside BOAZMAN. 9/28

Pin Swap. 10/05

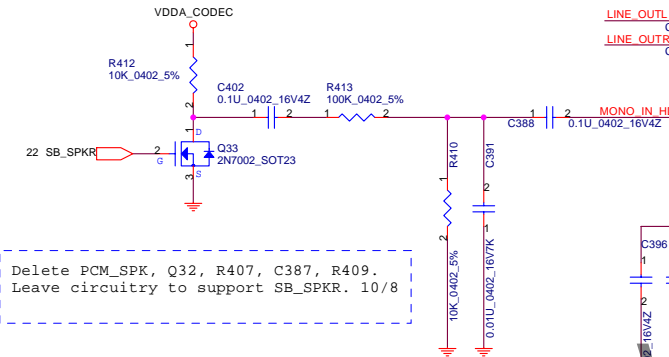
Swap P & N. 10/09



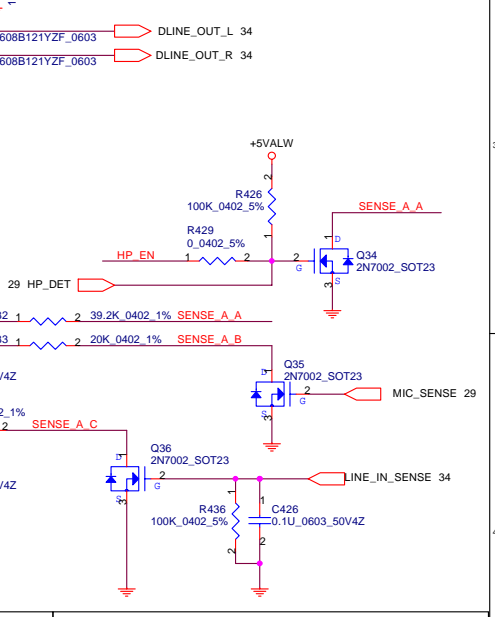
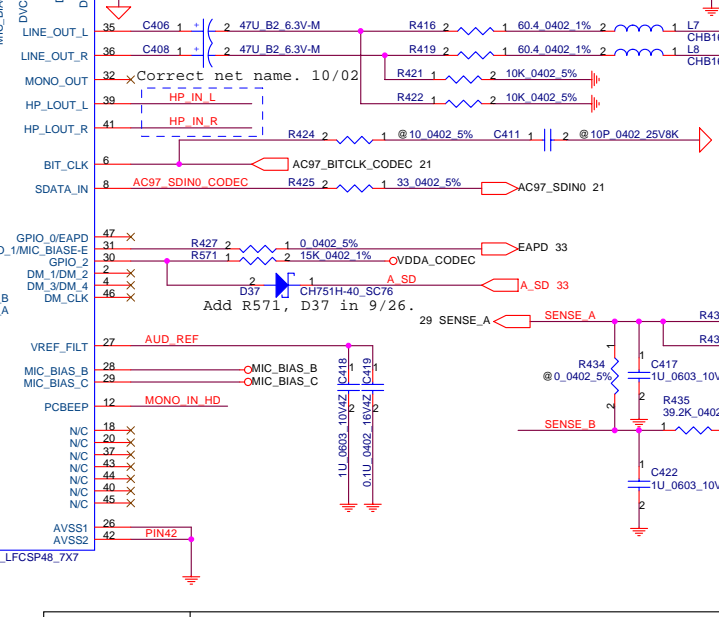
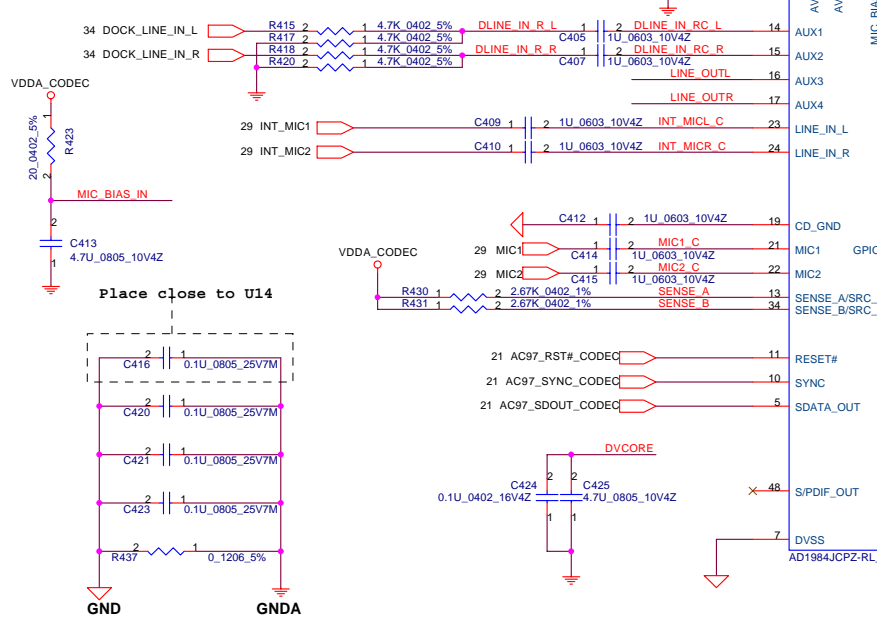
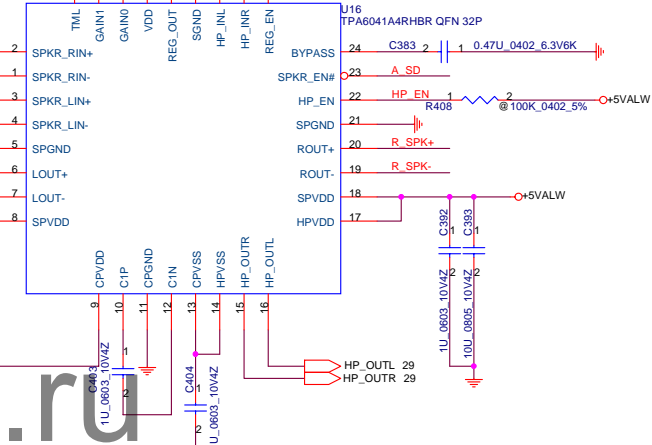
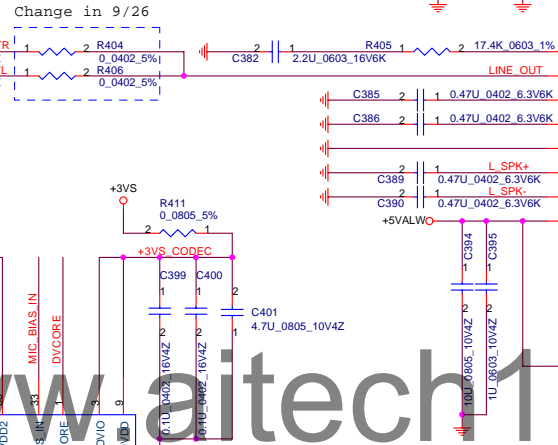
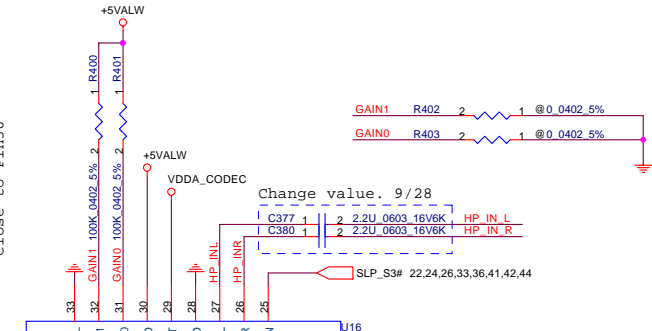
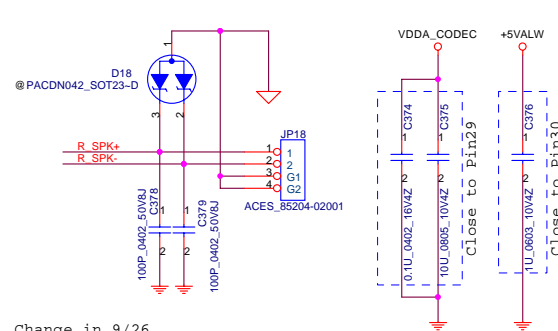
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Issued Date	2006/02/13	Deciphered Date	2006/07/26	Title	
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				Date: Monday, October 29, 2007	Sheet 25 of 45

AMP. FOR INTERNAL SPEAKER

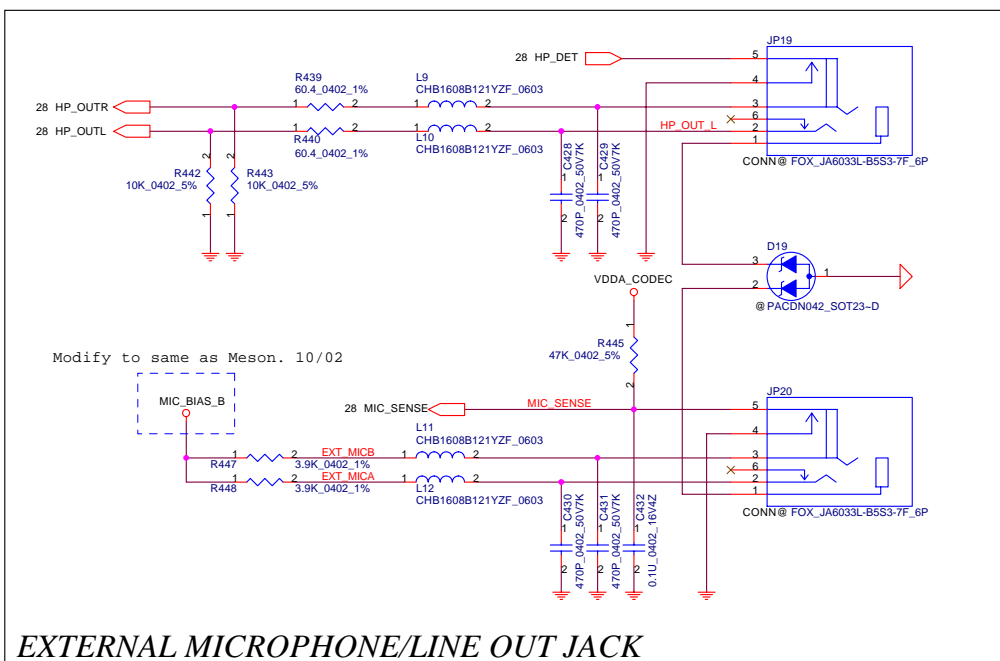
TPA6044 no longer needed. So delete BOM options & co-layout components for TPA6044. SGND and SGND1 nets can also be deleted. Only TPA6041 will be supported. 9/5



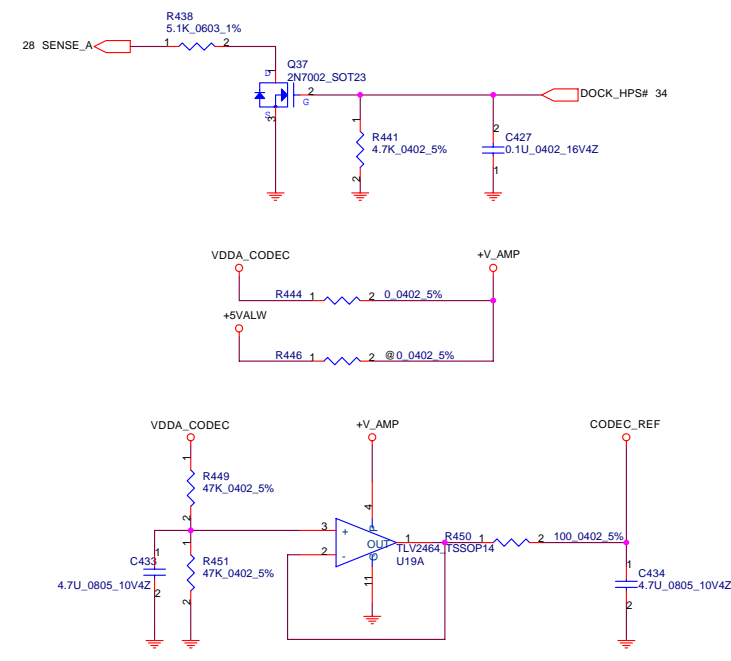
Delete PCM_SPK, Q32, R407, C387, R409. Leave circuitry to support SB_SPKR. 10/8



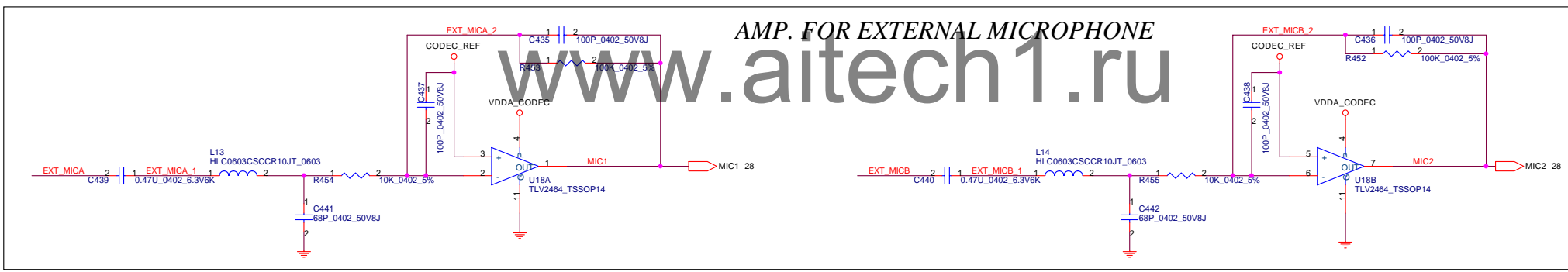
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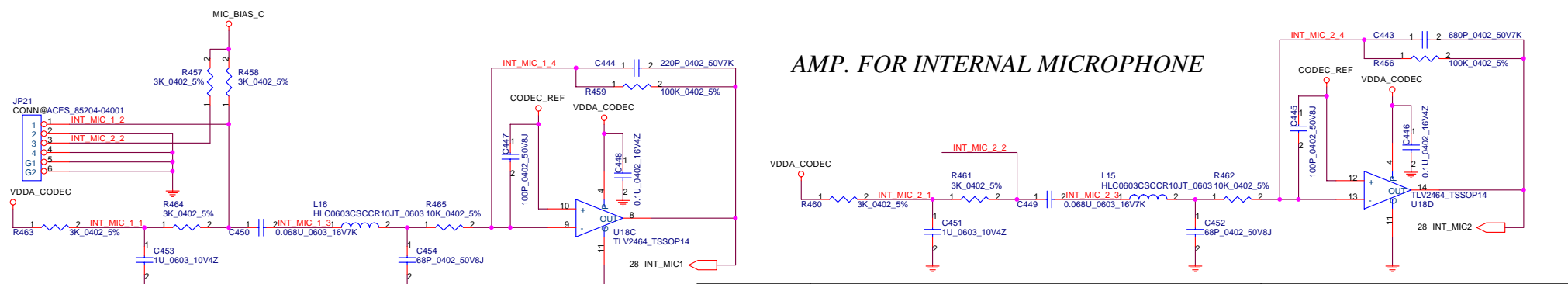
EXTERNAL MICROPHONE/LINE OUT JACK



AMP. FOR EXTERNAL MICROPHONE



AMP. FOR INTERNAL MICROPHONE



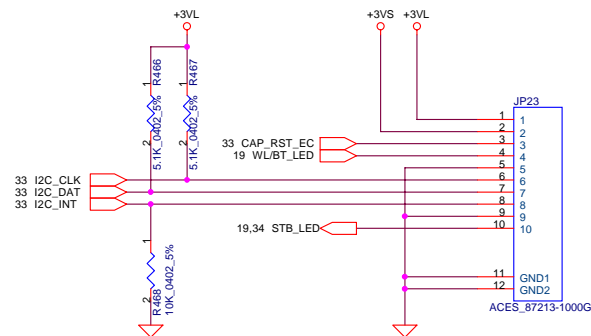
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Date: Monday, October 29, 2007				Sheet 29 of 45

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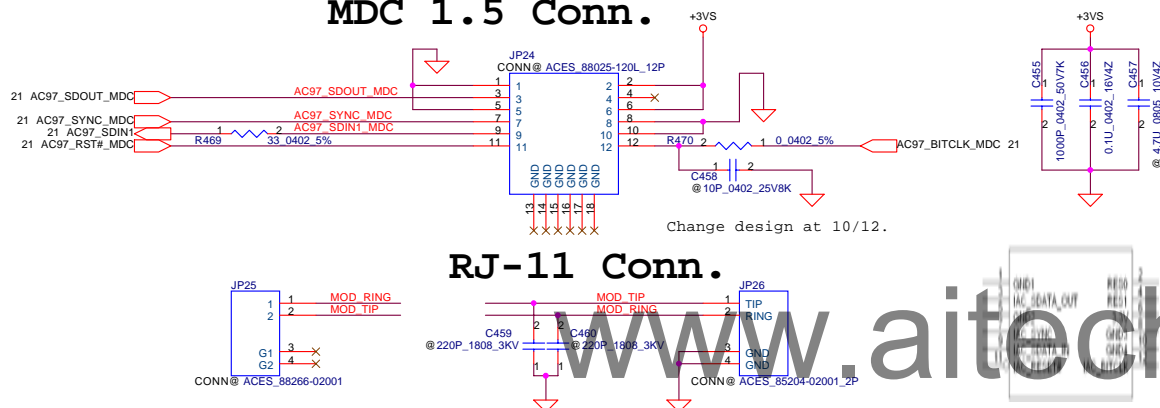
AMP & Audio Jack

Size Document Number LA-4021P Rev 0.1

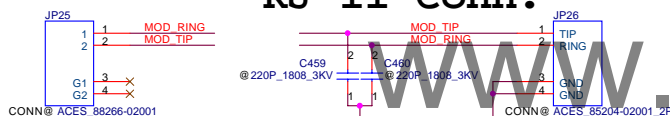
SWITCH BOARD.



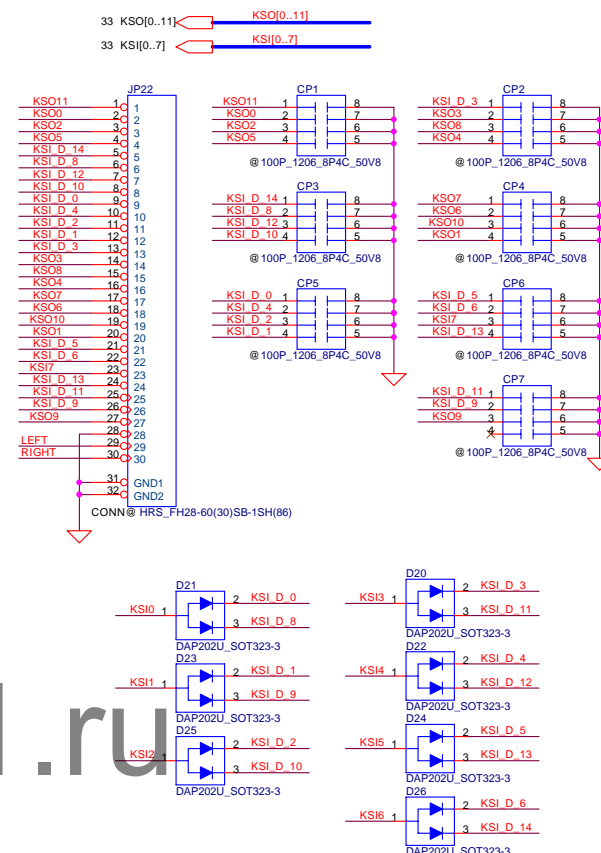
MDC 1.5 Conn.



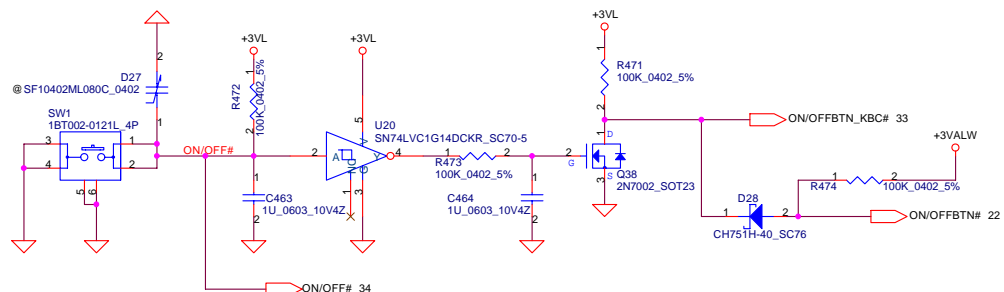
RJ-11 Conn.



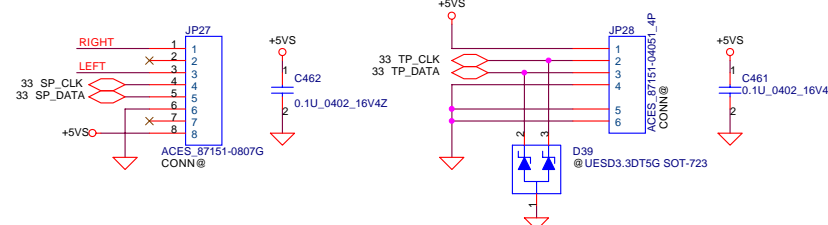
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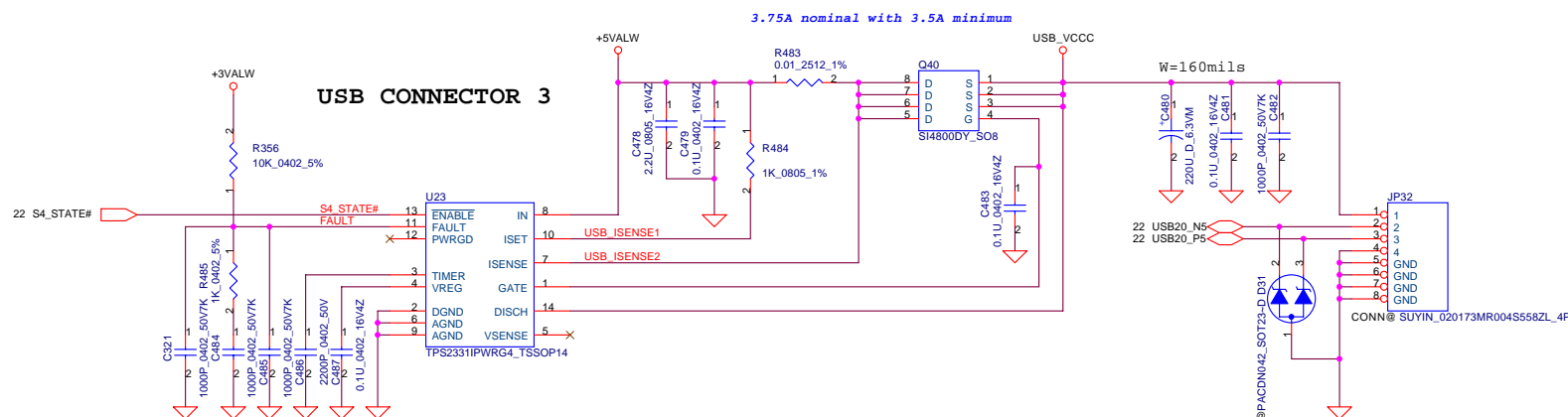
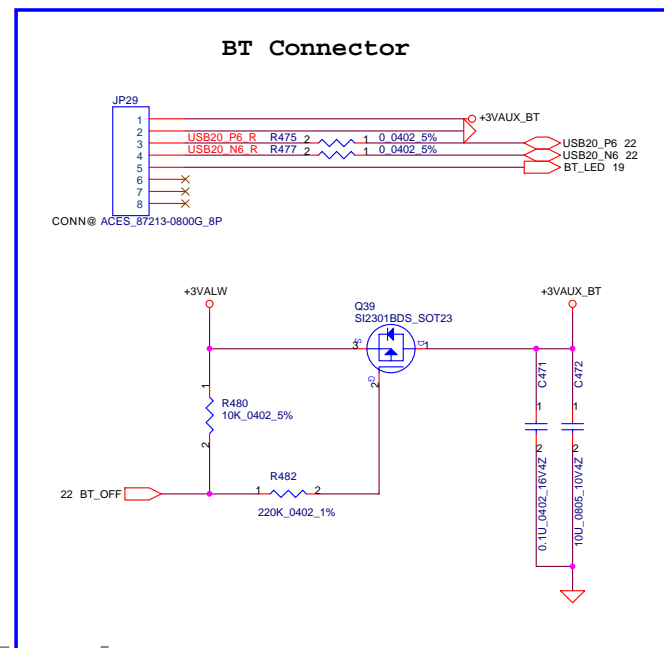
Power button



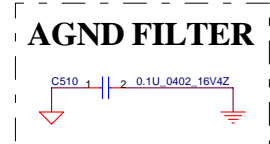
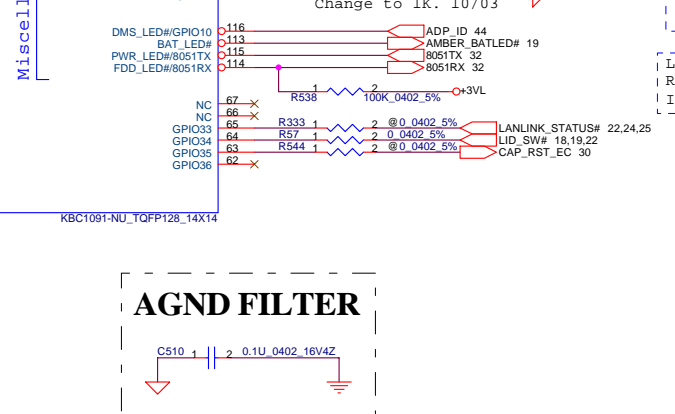
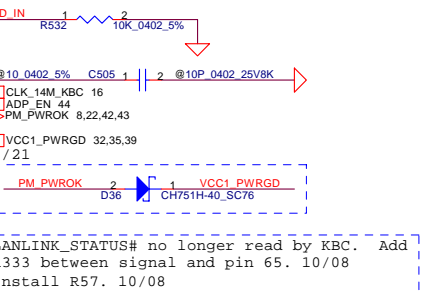
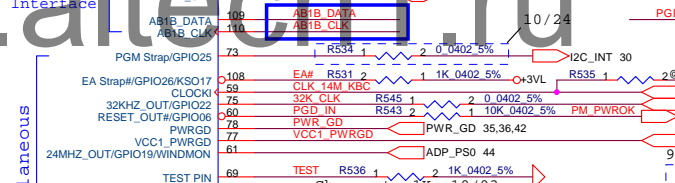
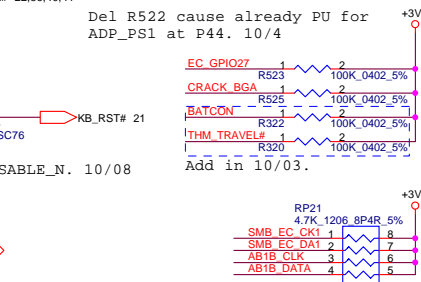
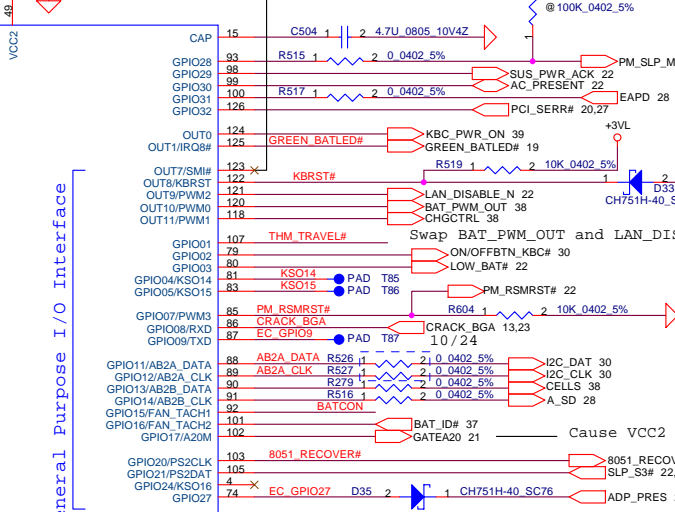
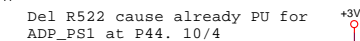
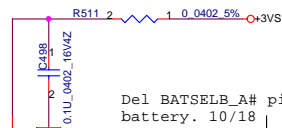
TrackPoint CONN. T/P BOARD.



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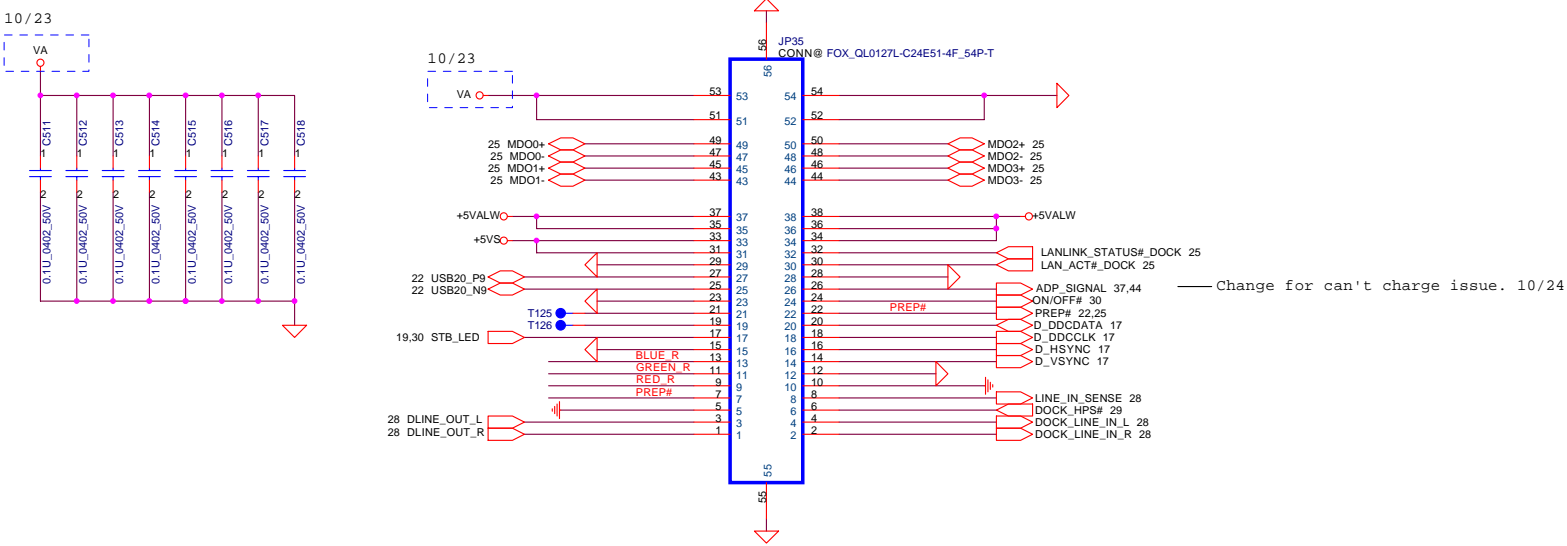


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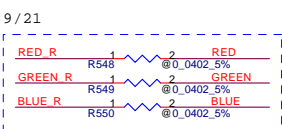
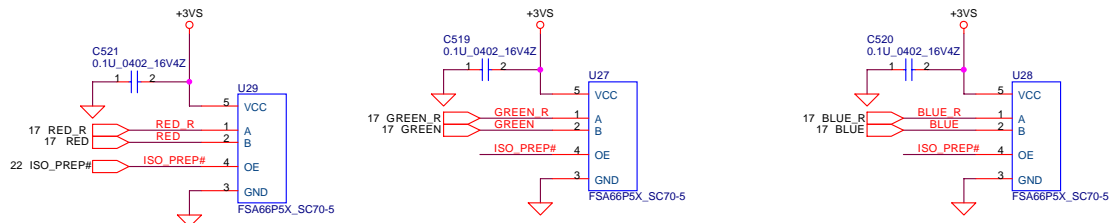


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				Date:	Monday, October 29, 2007	
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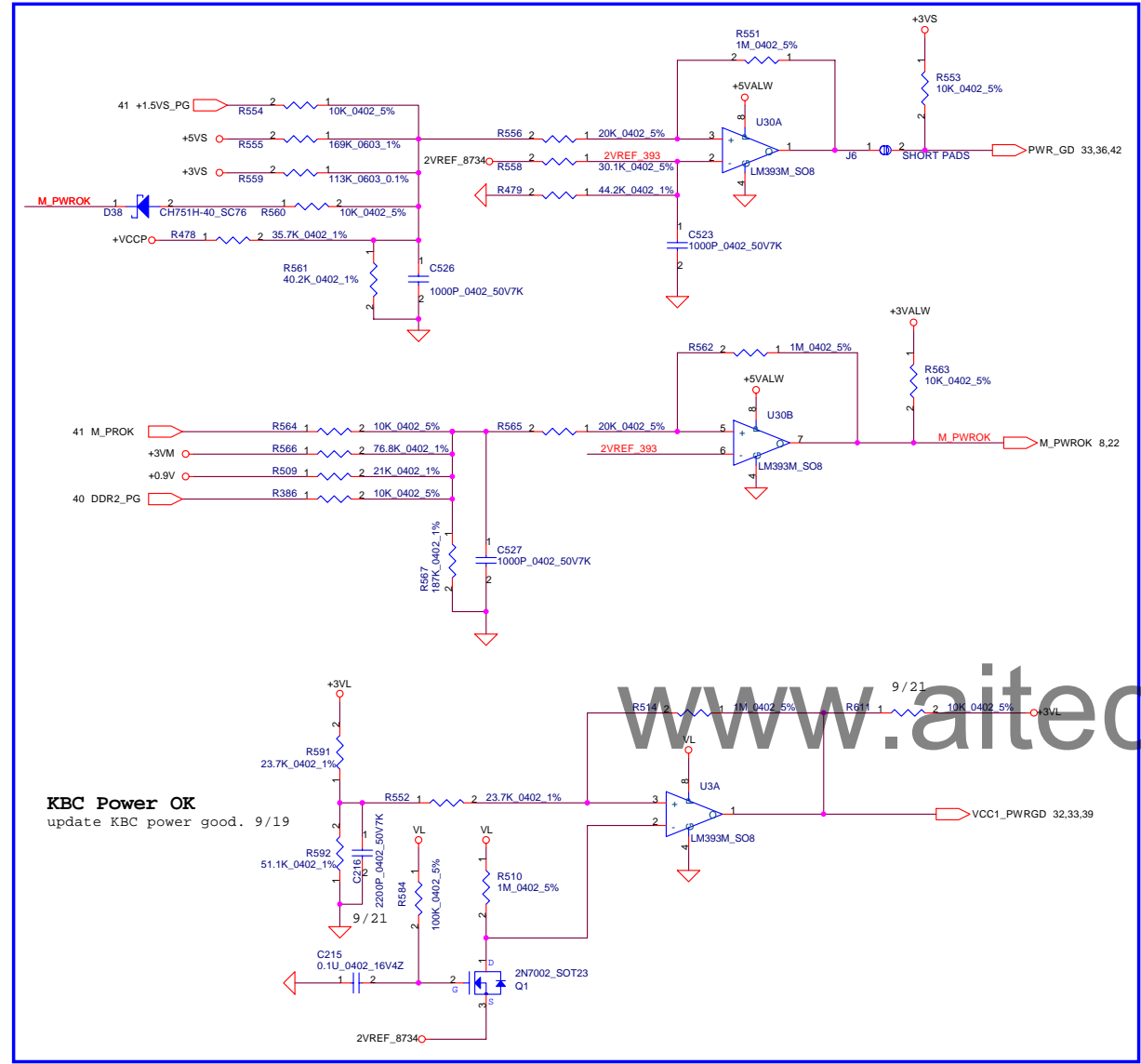
DOCKING CONNECT



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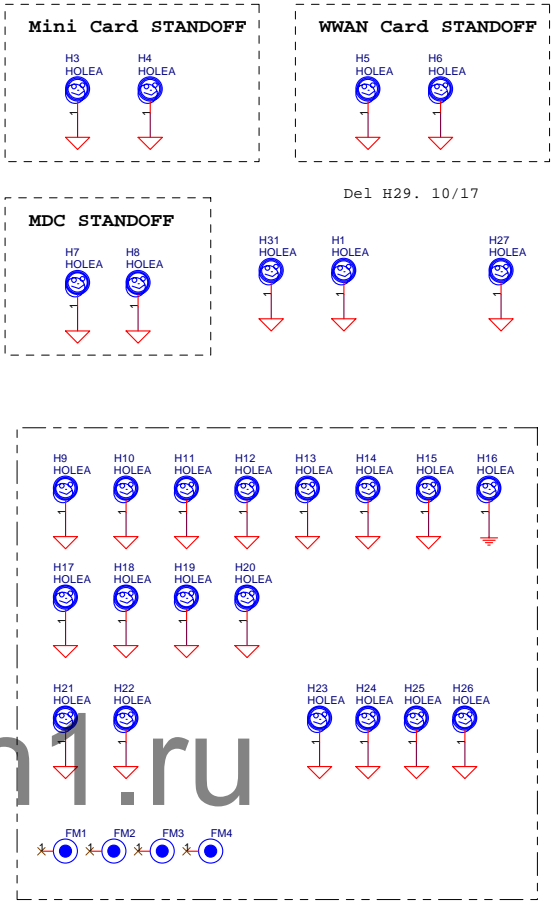


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KBC Power OK

update KBC power good. 9/19

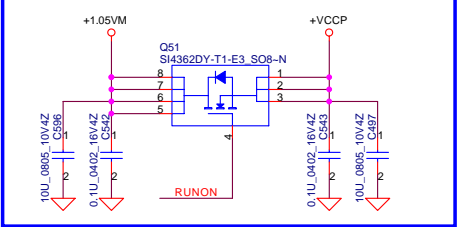


Del LAN reset schematic. 9/26

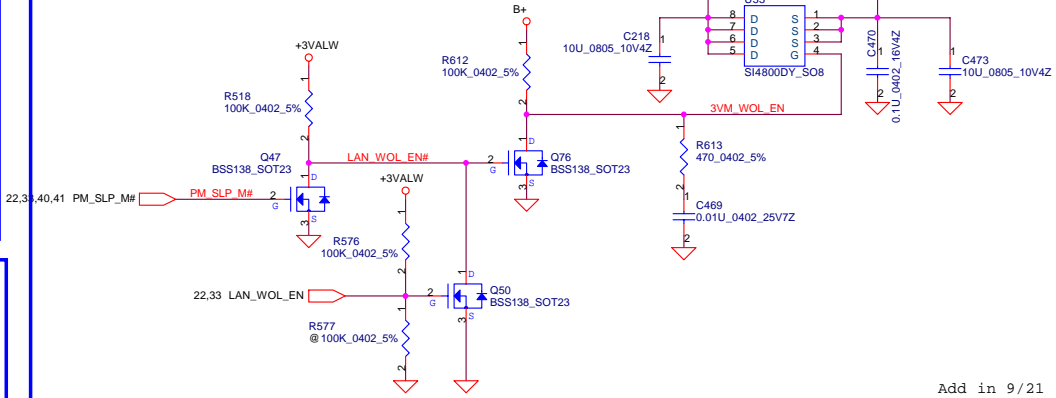
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				Monday, October 29, 2007	
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Modify at 7/31 after discuss with power team.

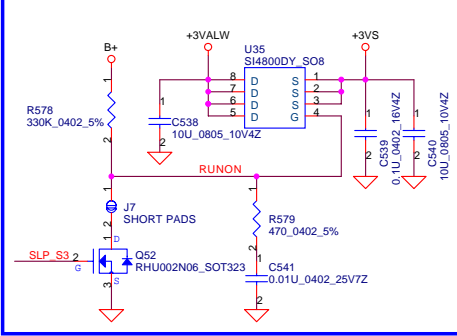
+1.05VM to +VCCP Transfer



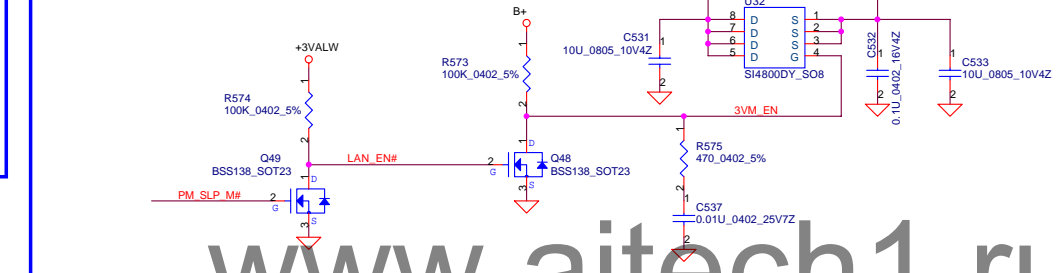
+3VALW to +3VM_WOL Transfer



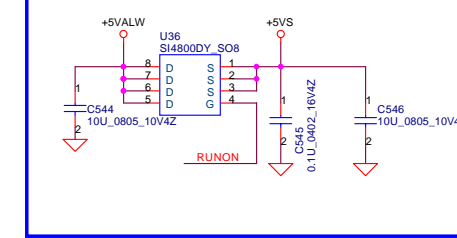
+3VALW to +3VS Transfer



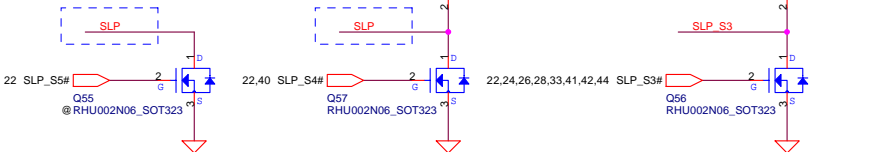
+3VALW to +3VM Transfer



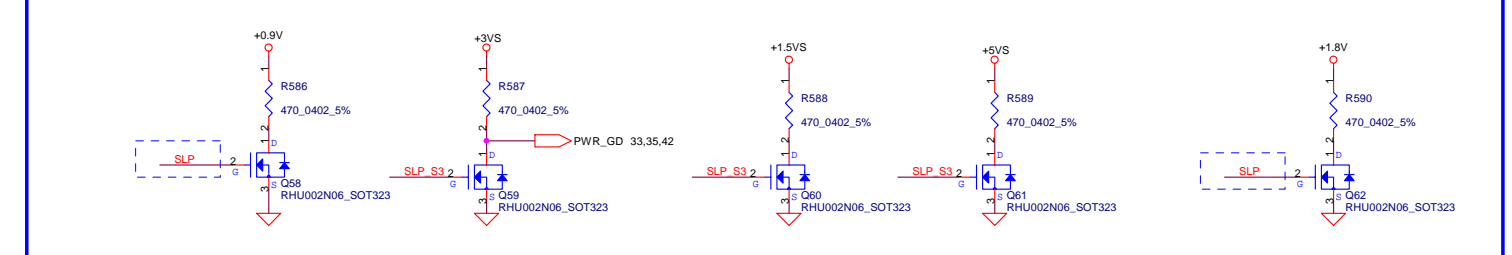
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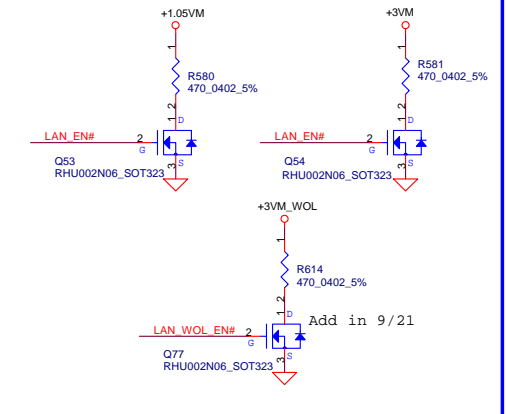
Design Change at 9/14.



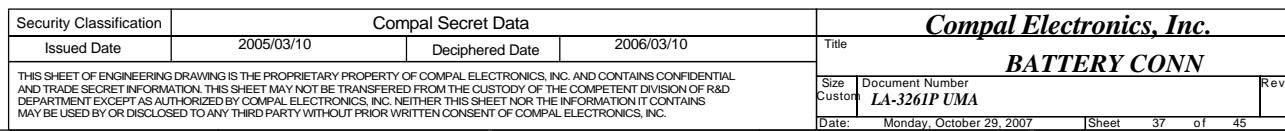
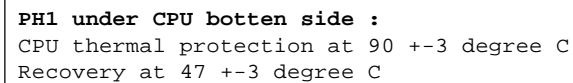
Discharge circuit-1

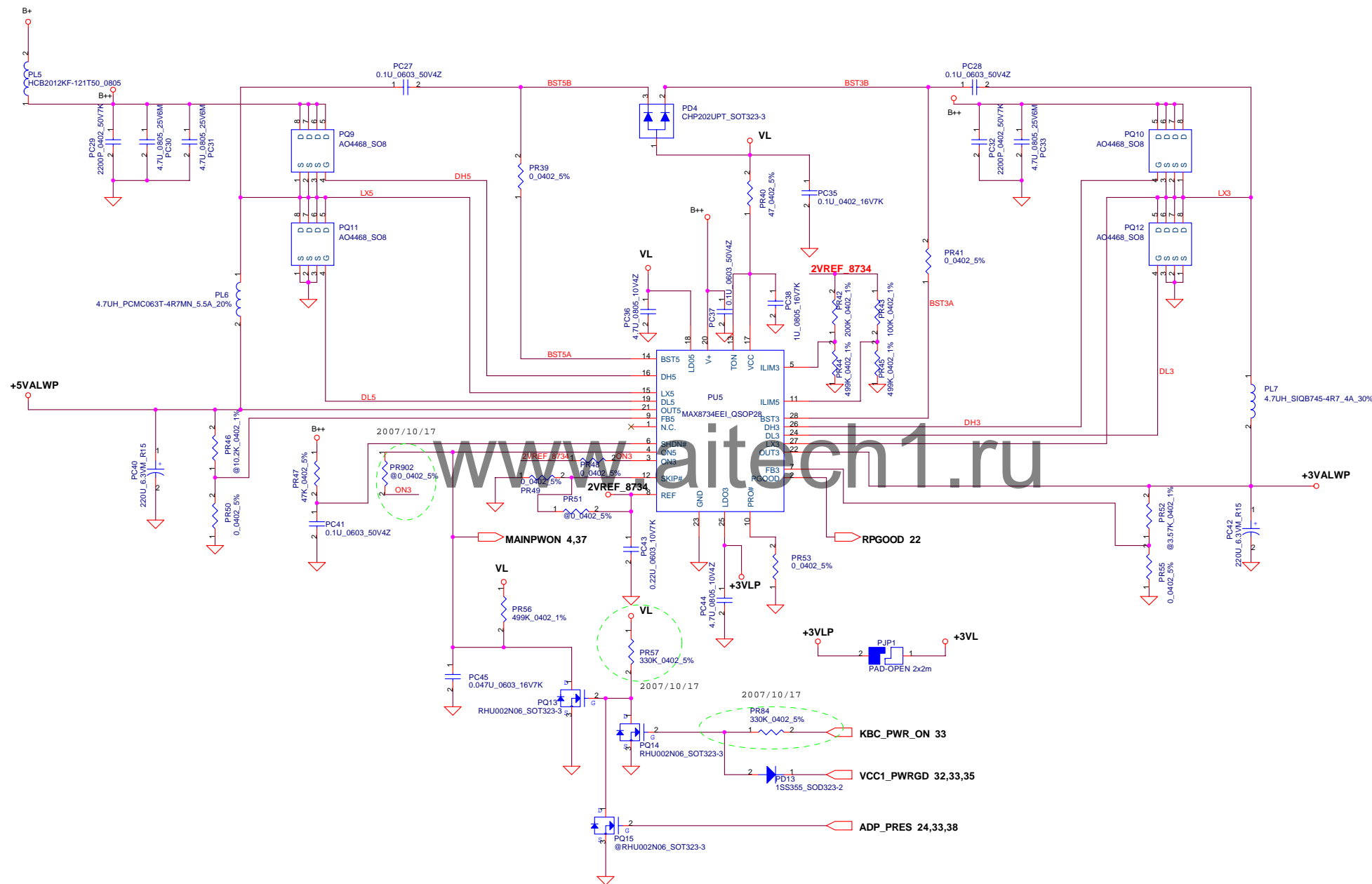


Discharge circuit-2 for V-M

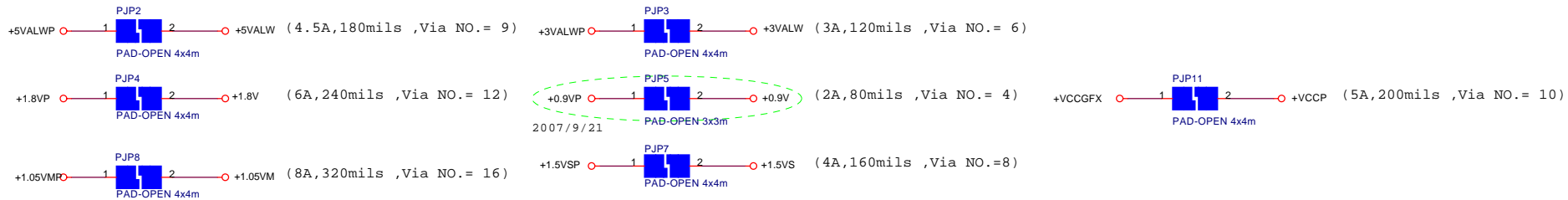
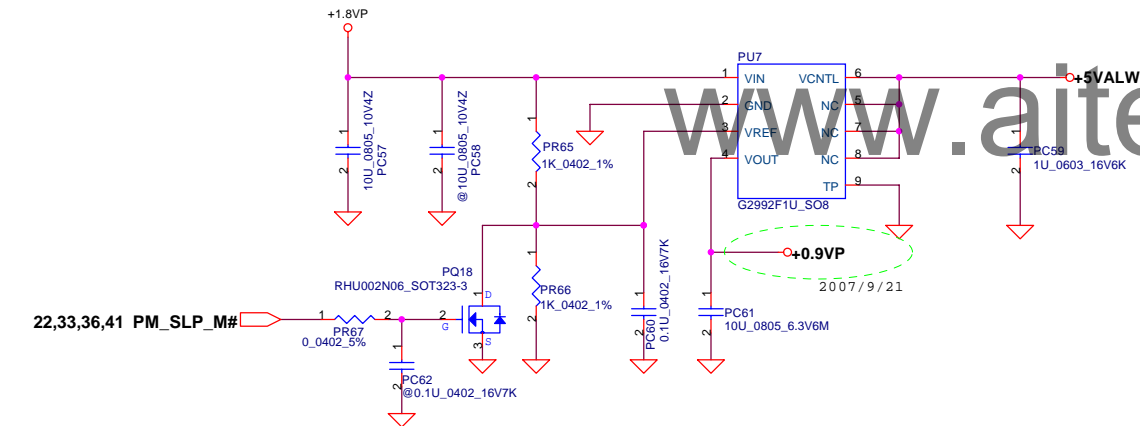
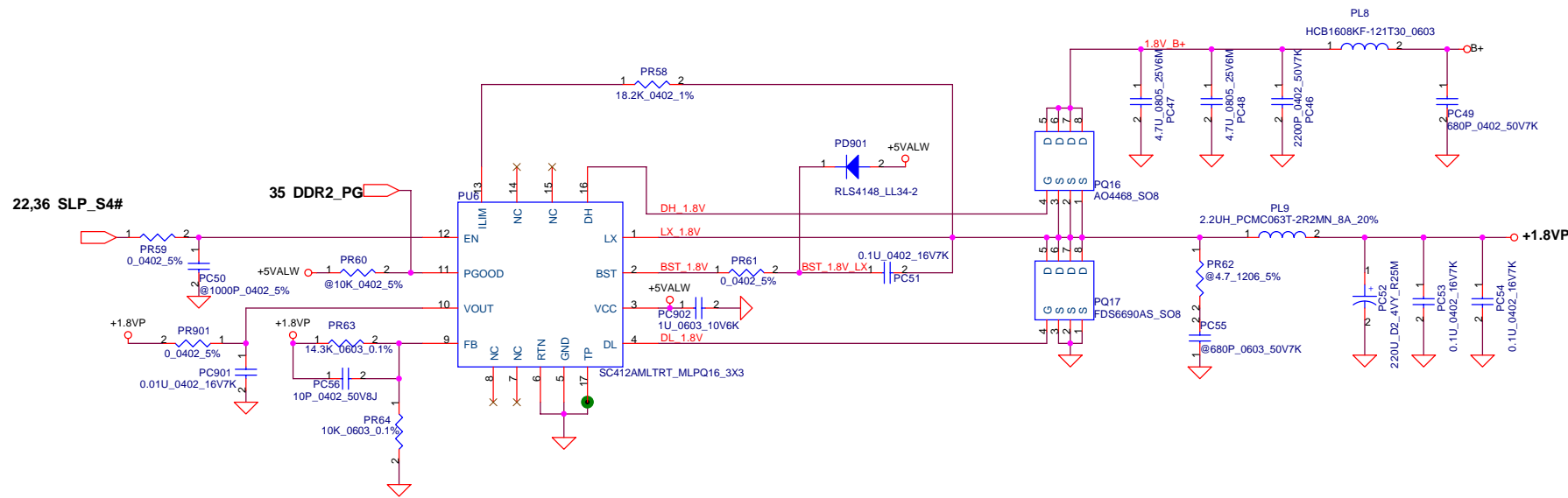


SYS. STATE	PM_SLP_M#	LAN_WOL_EN	+3VM_WOL	+3VM
M-off / No WOL	0	0	0V	0V
M-off / WOL	0	1	3.3V	0V
M1 (ME on)	1	0	3.3V	3.3V
M1 (ME on)	1	1	3.3V	3.3V

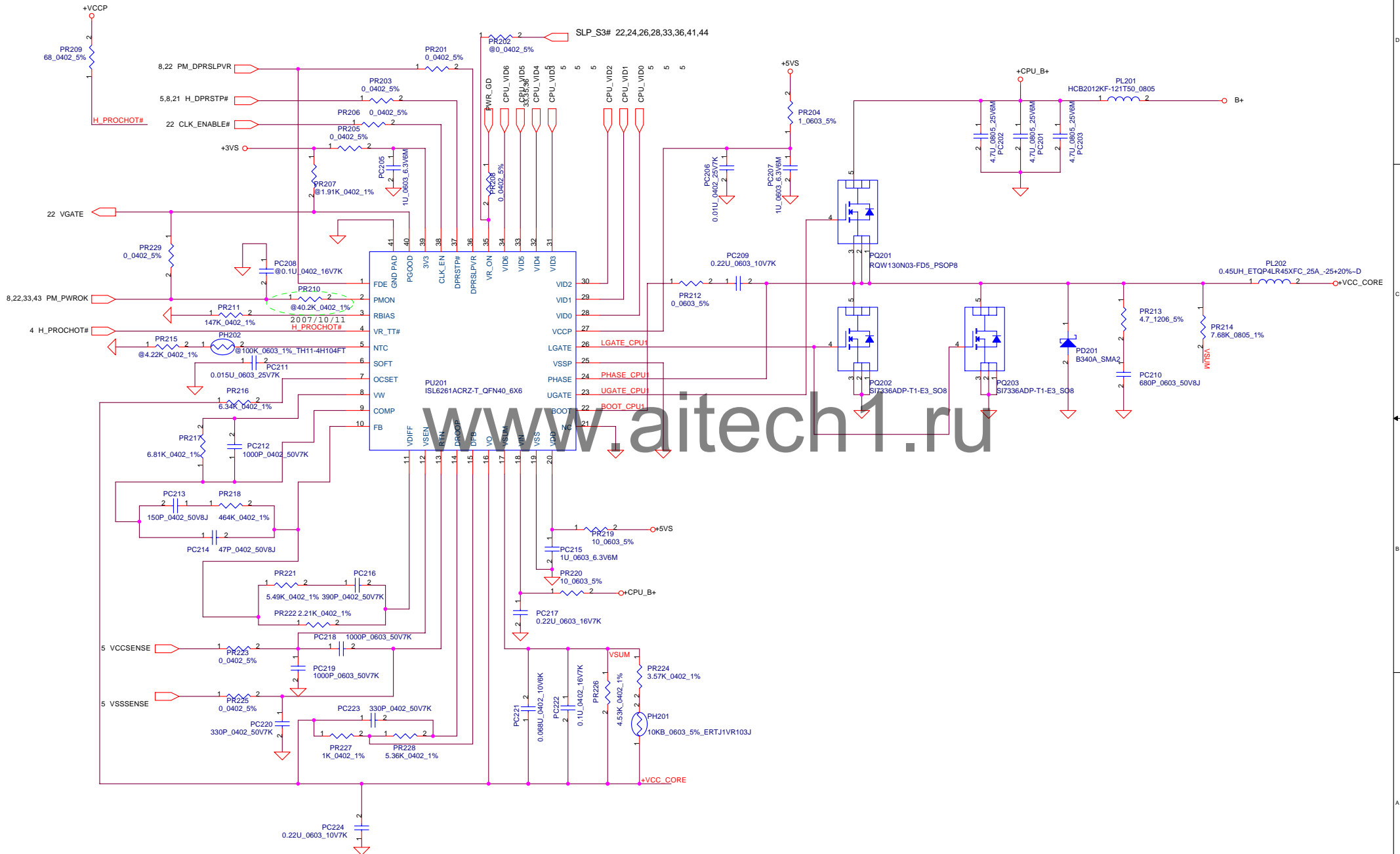




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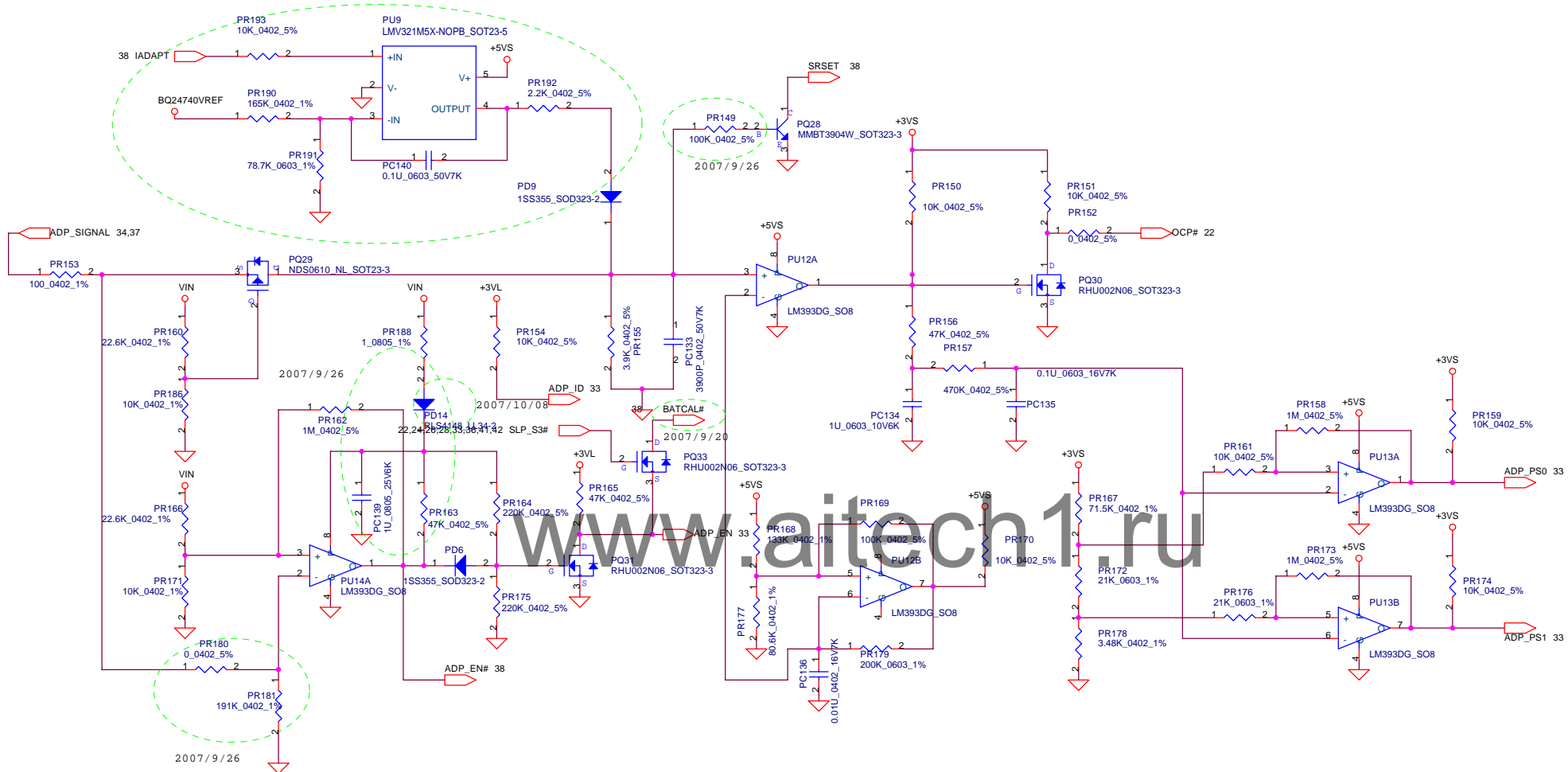


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<Title>		
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